

AV RECEIVER RX-V475/HTR-4066/ RX-V500D SERVICE MANUAL

RX-V475/HTR-4066 models

Note:

When the DIGITAL P.C.B. or IC22 on DIGITAL P.C.B. is replaced, this unit will display "Internal Error" and will not operate properly. The model name MUST be written to the backup IC (EEPROM: IC22 on DIGITAL P.C.B.) to have proper operation. (For details, refer to "S5. SOFT SWITCH" menu of the self-diagnostic function.)

注意:

DIGITAL P.C.B. または DIGITAL P.C.B. の IC22 を交換すると、"Internal Error" が表示されて本機が正常に動作しなくなります。正常に動作させるために、モデル名をバックアップ IC (EEPROM: DIGITAL P.C.B. の IC22) へ書き込む必要があります。(詳細は、ダイアグの "S5. SOFT SWITCH" メニューを参照してください。)

IMPORTANT NOTICE

This manual has been provided for the use of authorized Yamaha Retailers and their service personnel.

It has been assumed that basic service procedures inherent to the industry, and more specifically Yamaha Products, are already known and understood by the users, and have therefore not been restated.

WARNING: Failure to follow appropriate service and safety procedures when servicing this product may result in personal injury, destruction of expensive components, and failure of the product to perform as specified. For these reasons, we advise all Yamaha product owners that any service required should be performed by an authorized Yamaha Retailer or the appointed service representative.

IMPORTANT: The presentation or sale of this manual to any individual or firm does not constitute authorization, certification or recognition of any applicable technical capabilities, or establish a principle-agent relationship of any form.

The data provided is believed to be accurate and applicable to the unit(s) indicated on the cover. The research, engineering, and service departments of Yamaha are continually striving to improve Yamaha products. Modifications are, therefore, inevitable and specifications are subject to change without notice or obligation to retrofit. Should any discrepancy appear to exist, please contact the distributor's Service Division.

WARNING: Static discharges can destroy expensive components. Discharge any static electricity your body may have accumulated by grounding yourself to the ground buss in the unit (heavy gauge black wires connect to this buss).

IMPORTANT: Turn the unit OFF during disassembly and part replacement. Recheck all work before you apply power to the unit.

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■ TO SERVICE PERSONNEL

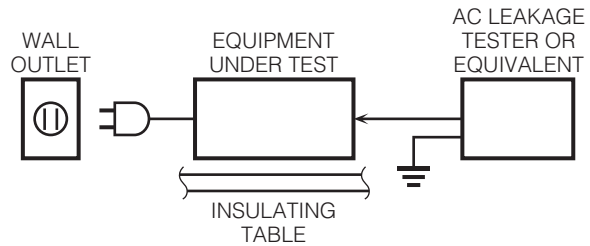
1. Critical Components Information

Components having special characteristics are marked Δ and must be replaced with parts having specifications equal to those originally installed.

2. Leakage Current Measurement (For 120V Models Only)

When service has been completed, it is imperative to verify that all exposed conductive surfaces are properly insulated from supply circuits.

- Meter impedance should be equivalent to 1500 ohms shunted by 0.15 μ F.



- Leakage current must not exceed 0.5mA.
- Be sure to test for leakage with the AC plug in both polarities.



For U model

“CAUTION”

“F5401: FOR CONTINUED PROTECTION AGAINST RISK OF FIRE, REPLACE ONLY WITH SAME TYPE 2A, 250V FUSE.”

“F5402: FOR CONTINUED PROTECTION AGAINST RISK OF FIRE, REPLACE ONLY WITH SAME TYPE 6A, 125V FUSE.”

For C model

CAUTION

F5401: REPLACE WITH SAME TYPE 2A, 250V FUSE.

F5402: REPLACE WITH SAME TYPE 6A, 125V FUSE.

ATTENTION

F5401: UTILISER UN FUSIBLE DE RECHANGE DE MÊME TYPE DE 2A, 250V.

F5402: UTILISER UN FUSIBLE DE RECHANGE DE MÊME TYPE DE 6A, 125V.

WARNING: CHEMICAL CONTENT NOTICE!

This product contains chemicals known to the State of California to cause cancer, or birth defects or other reproductive harm.

DO NOT PLACE SOLDER, ELECTRICAL/ELECTRONIC OR PLASTIC COMPONENTS IN YOUR MOUTH FOR ANY REASON WHATSOEVER!

Avoid prolonged, unprotected contact between solder and your skin! When soldering, do not inhale solder fumes or expose eyes to solder/flux vapor!

If you come in contact with solder or components located inside the enclosure of this product, wash your hands before handling food.

About lead free solder / 無鉛ハンダについて

All of the P.C.B.s installed in this unit and solder joints are soldered using the lead free solder.

Among some types of lead free solder currently available, it is recommended to use one of the following types for the repair work.

- Sn + Ag + Cu (tin + silver + copper)
- Sn + Cu (tin + copper)
- Sn + Zn + Bi (tin + zinc + bismuth)

Caution:

As the melting point temperature of the lead free solder is about 30°C to 40°C (50°F to 70°F) higher than that of the lead solder, be sure to use a soldering iron suitable to each solder.

本機に搭載されているすべての基板およびハンダ付けによる接合部は無鉛ハンダでハンダ付けされています。

無鉛ハンダにはいくつかの種類がありますが、修理時には下記のような無鉛ハンダの使用を推奨します。

- Sn+Ag+Cu (錫 + 銀 + 銅)
- Sn+Cu (錫 + 銅)
- Sn+Zn+Bi (錫 + 亜鉛 + ビスマス)

注意：

無鉛ハンダの融点温度は通常の鉛入りハンダに比べ 30 ～ 40℃程度高くなっていますので、それぞれのハンダに合ったハンダごてをご使用ください。

FRONT PANELS

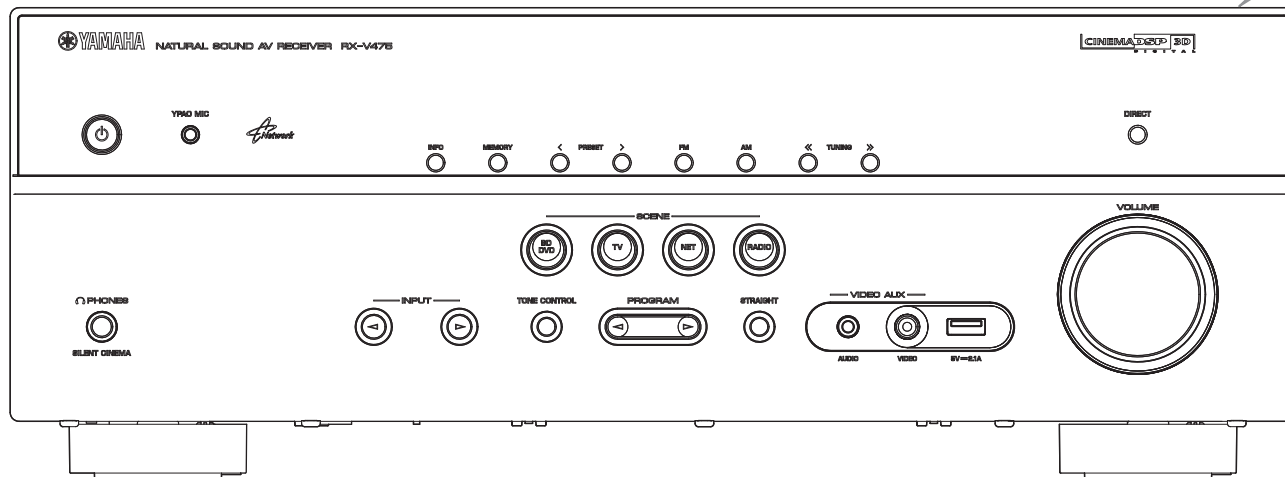
RX-V475

U, C, R, T, K, A, B, G, F, L, S, H models

*M-HL H-RTN dtkom X-PLY

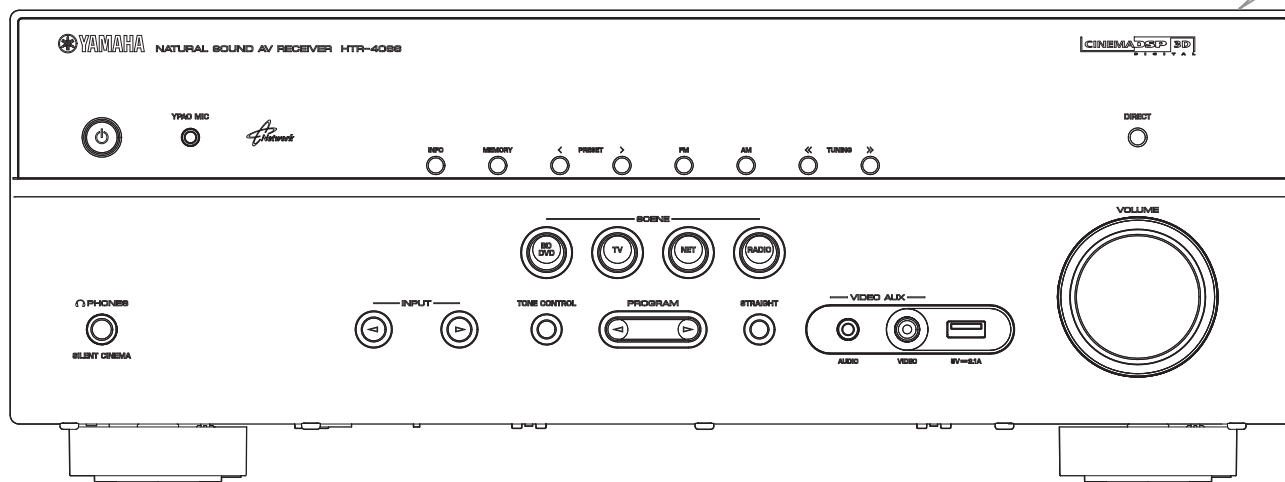
J model

*M-HL H-RTN dtkom X-PLY



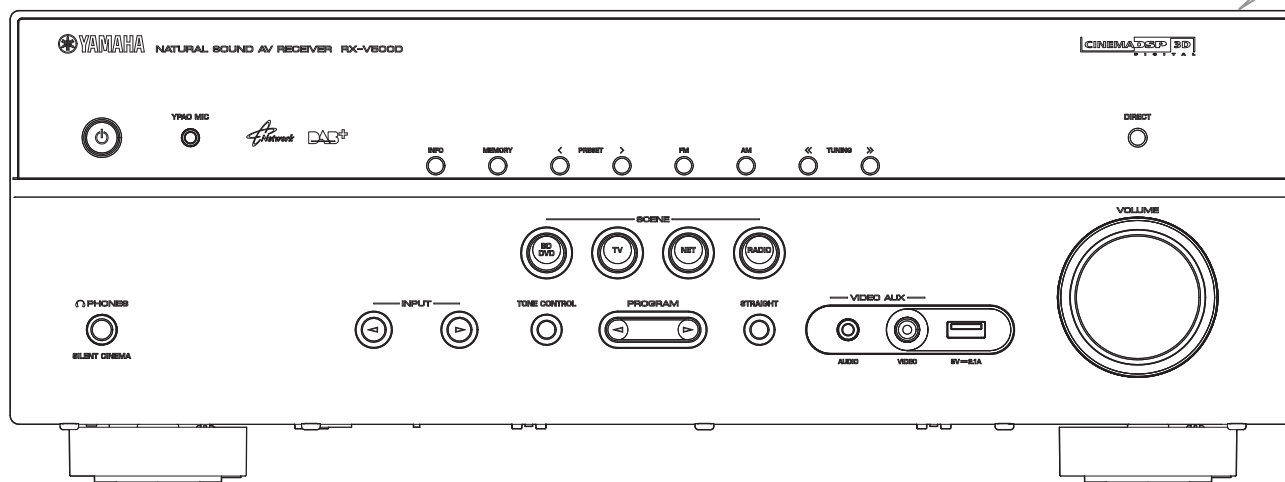
HTR-4066

*M-HL H-RTN dtkom X-PLY



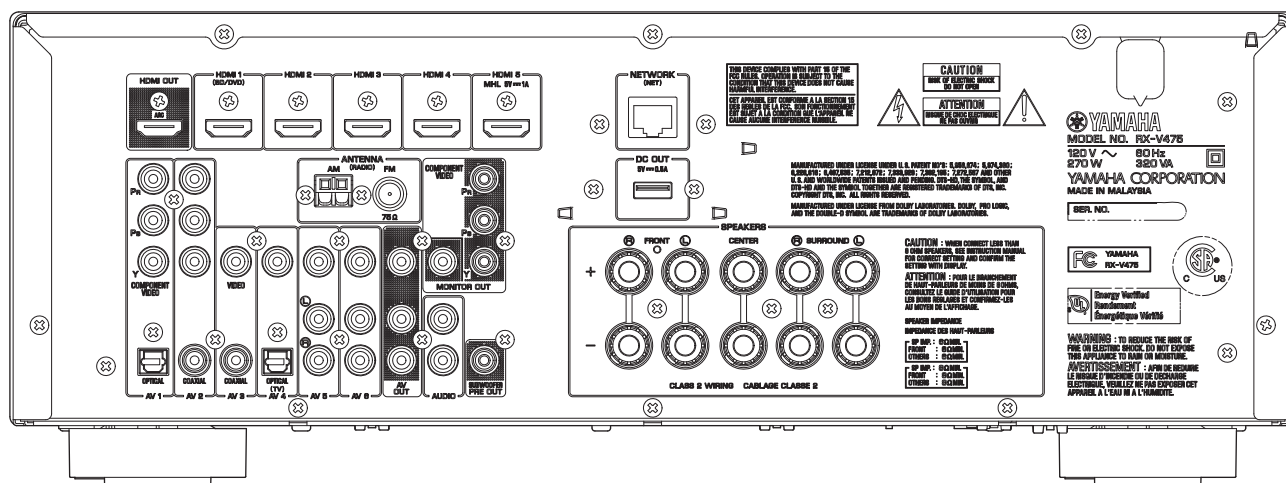
RX-V500D

*M-HL H-RTN dtkom X-PLY

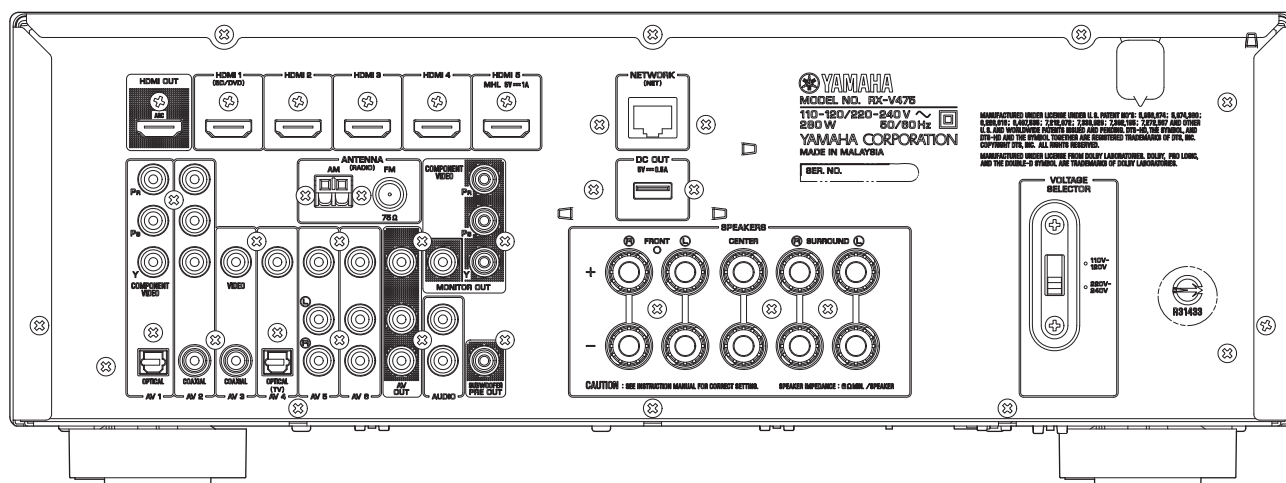


REAR PANELS

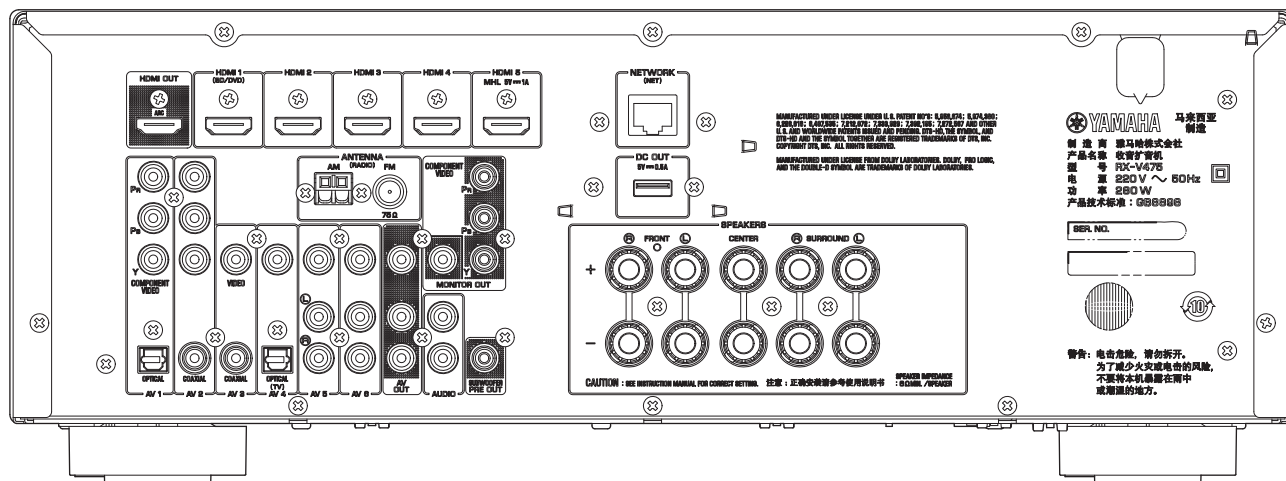
RX-V475 (U, C models)



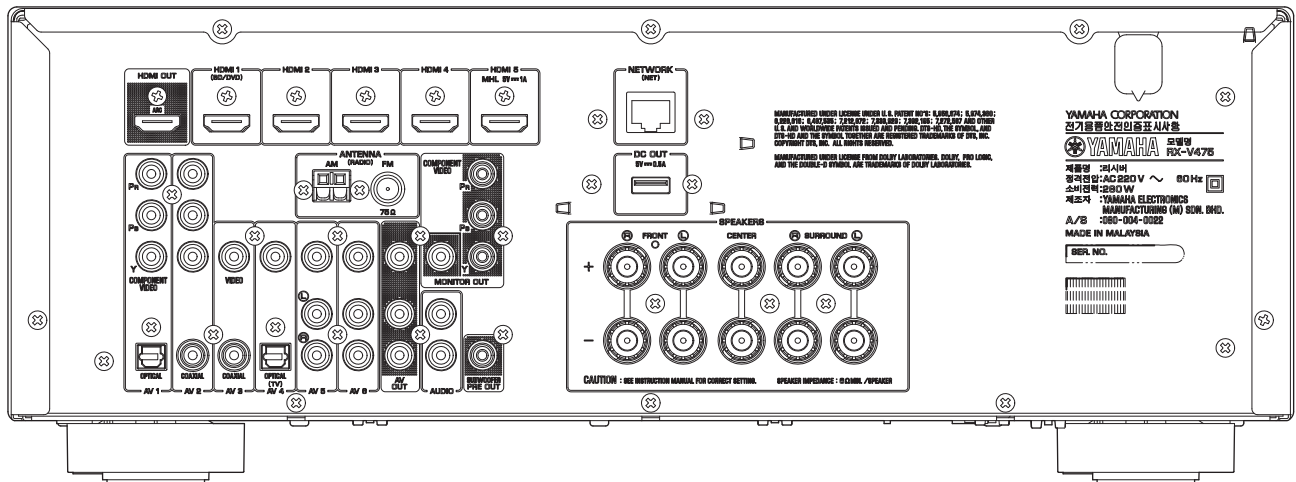
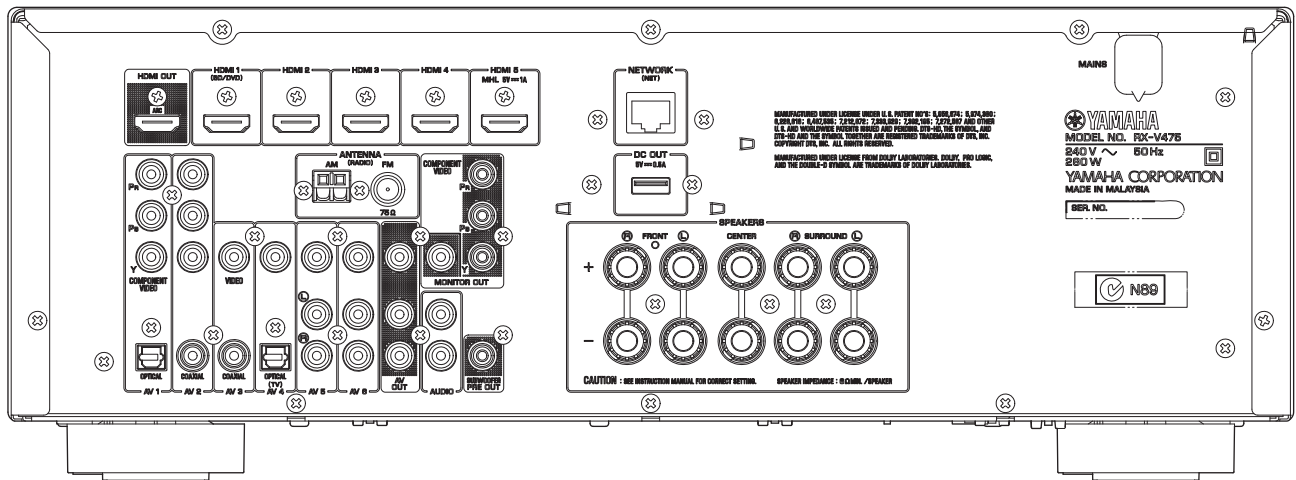
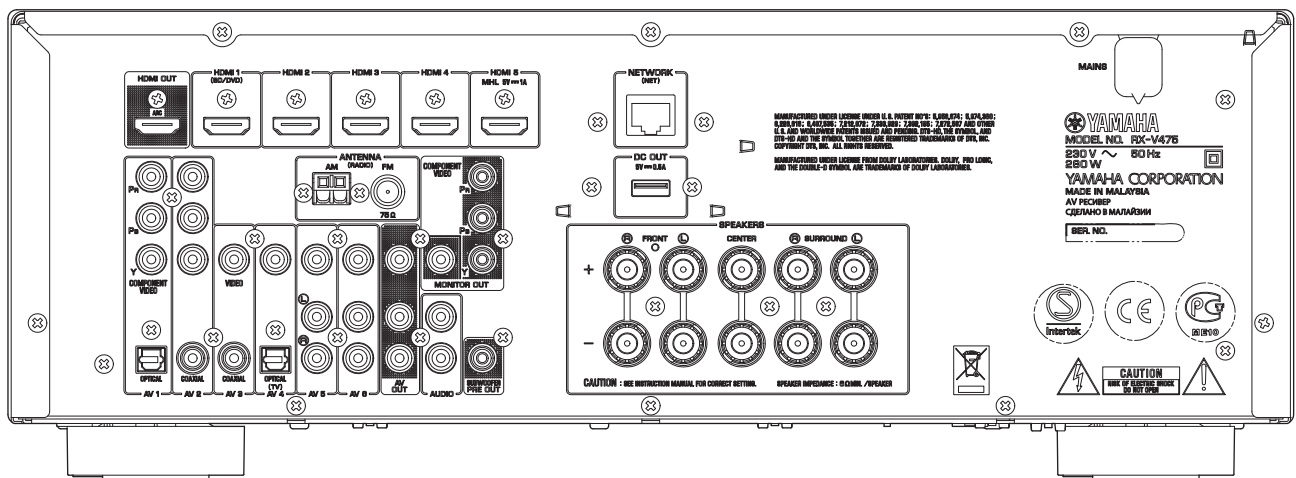
RX-V475 (R, S models)



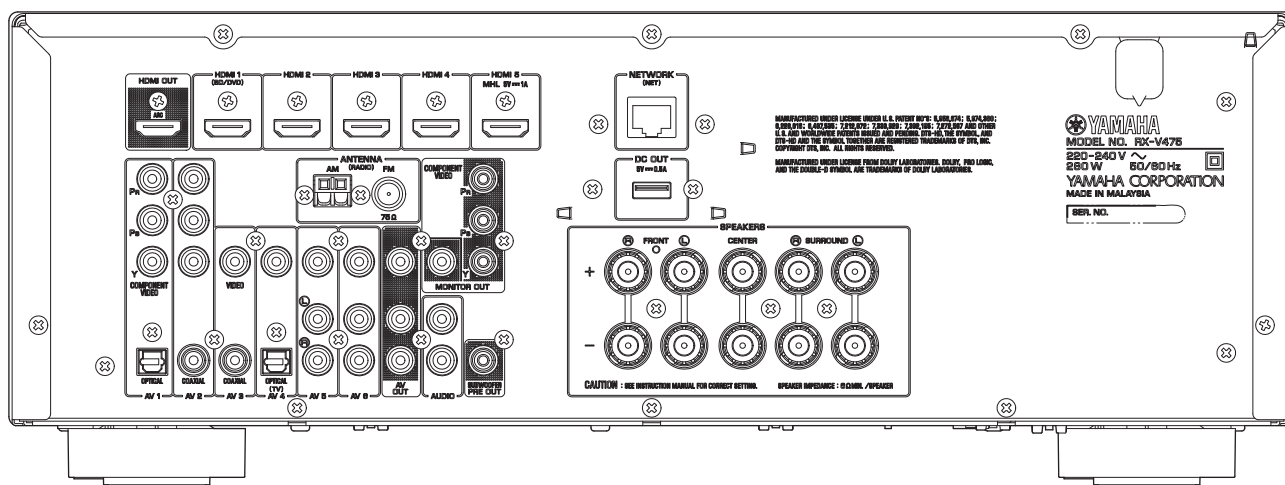
RX-V475 (T model)



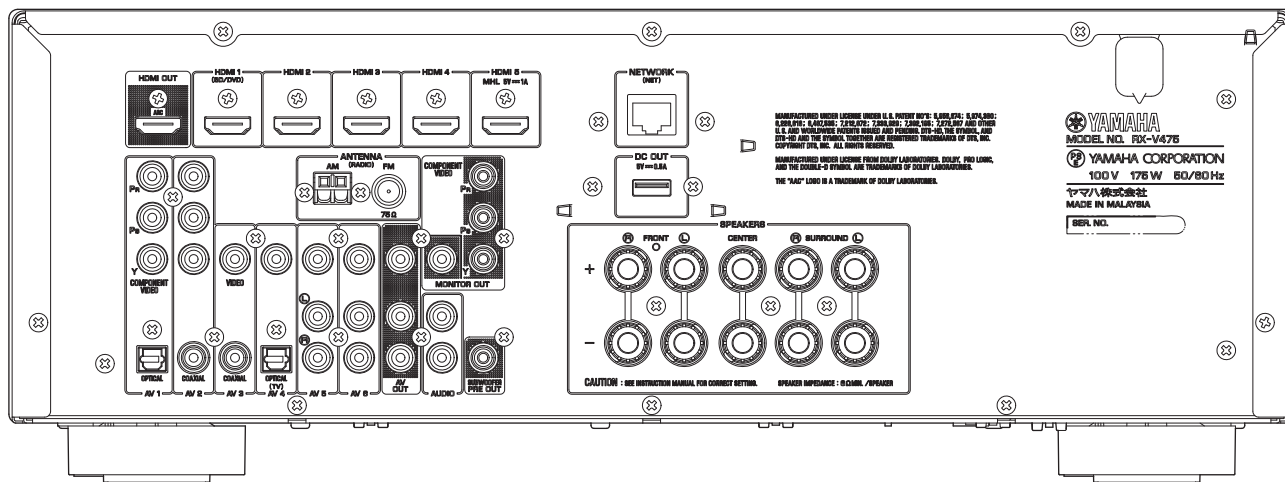
RX-V475 (K model)

**RX-V475 (A model)****RX-V475 (B, G, F models)**

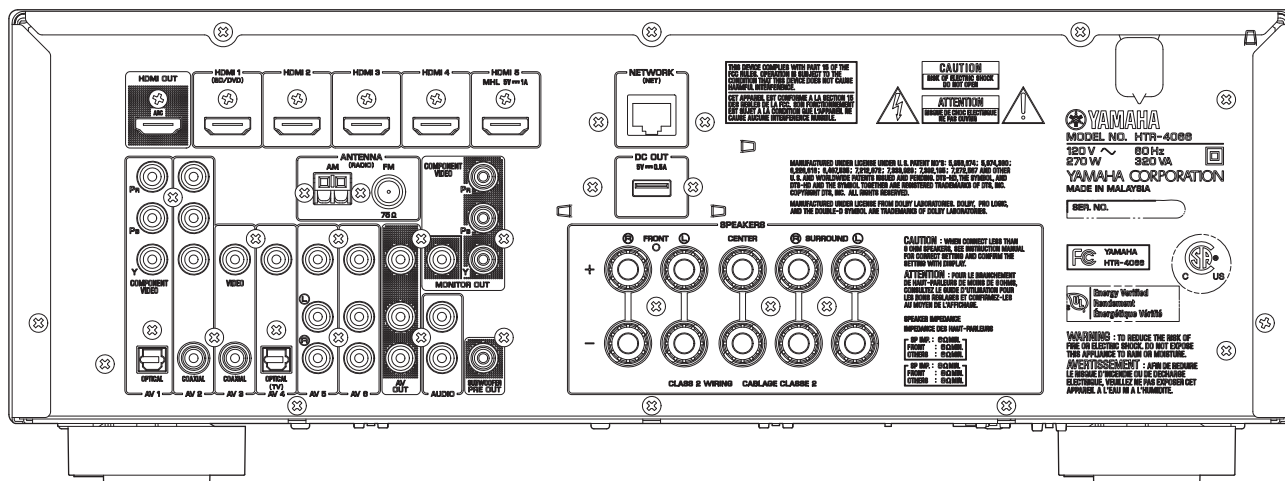
RX-V475 (L, H models)



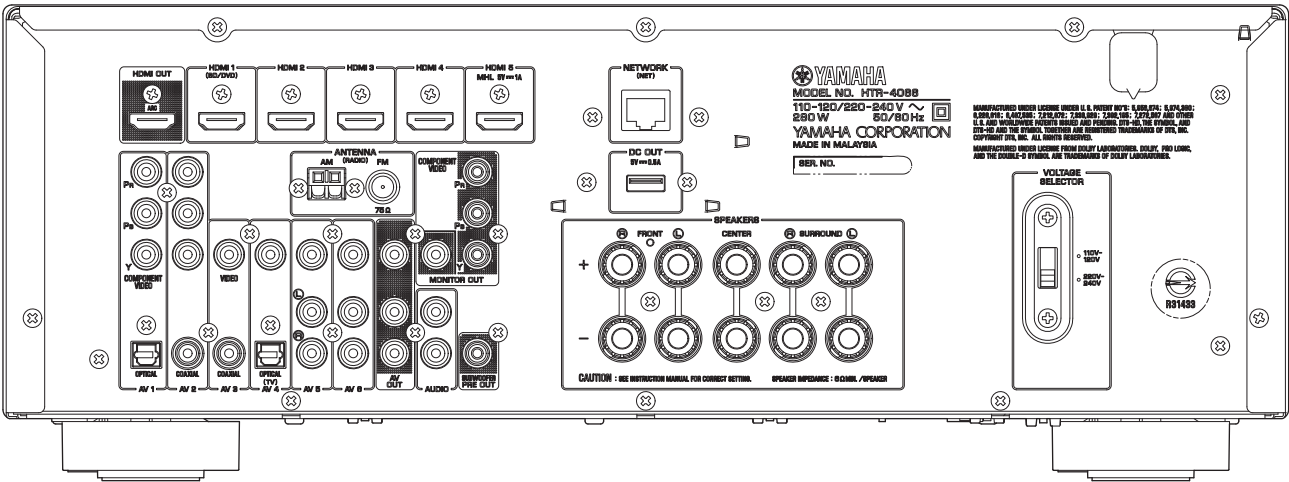
RX-V475 (J model)



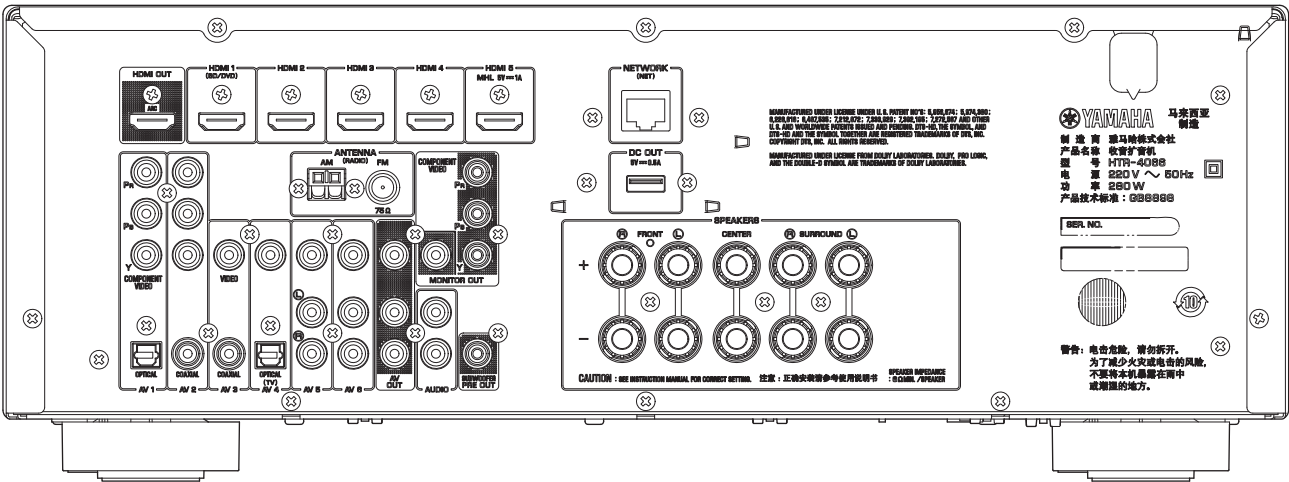
HTR-4066 (U model)



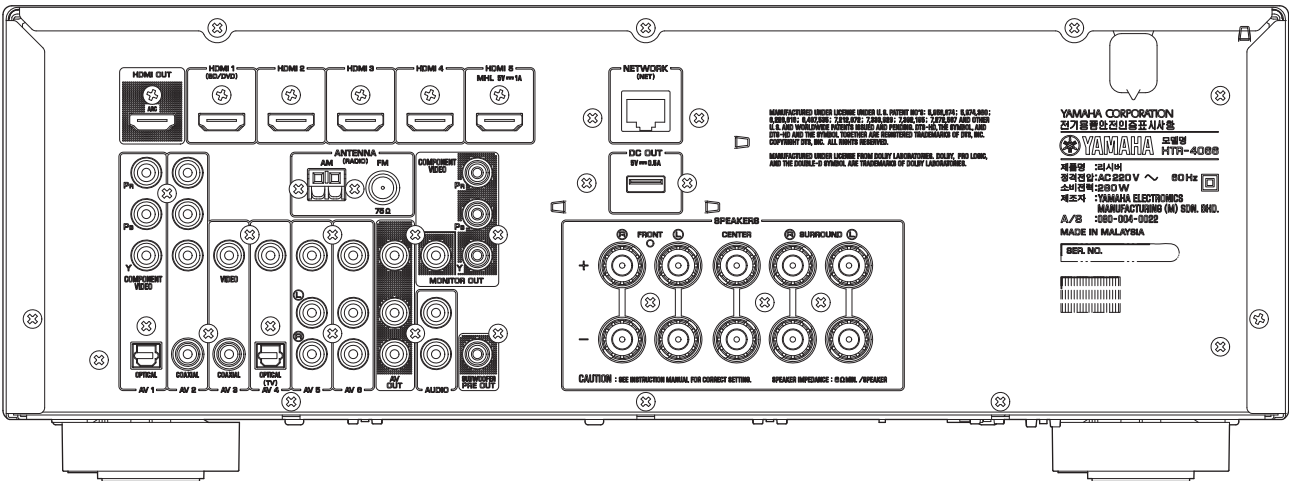
HTR-4066 (R model)



HTR-4066 (T model)

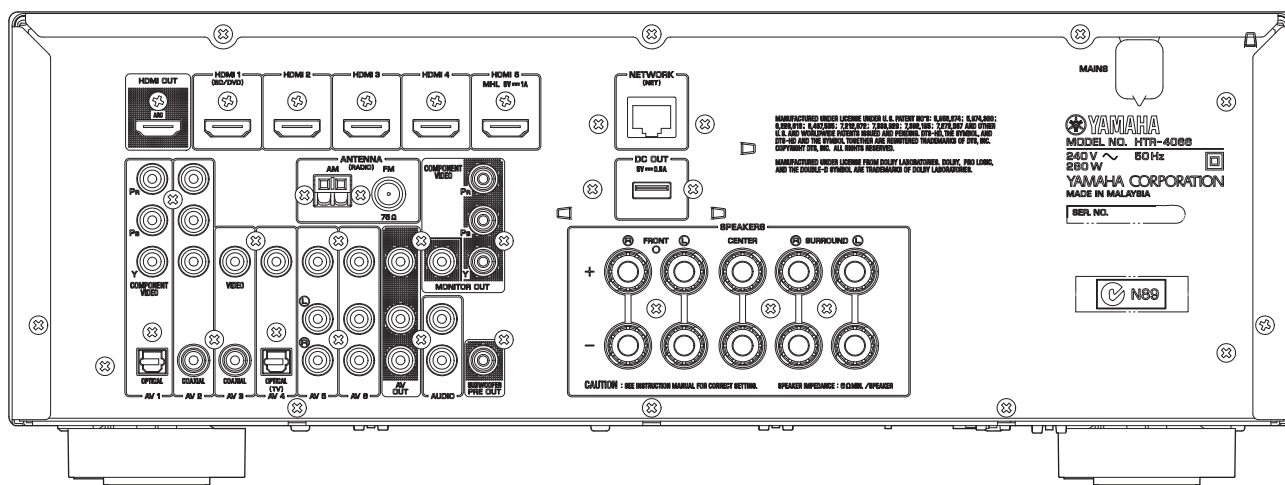


HTR-4066 (K model)

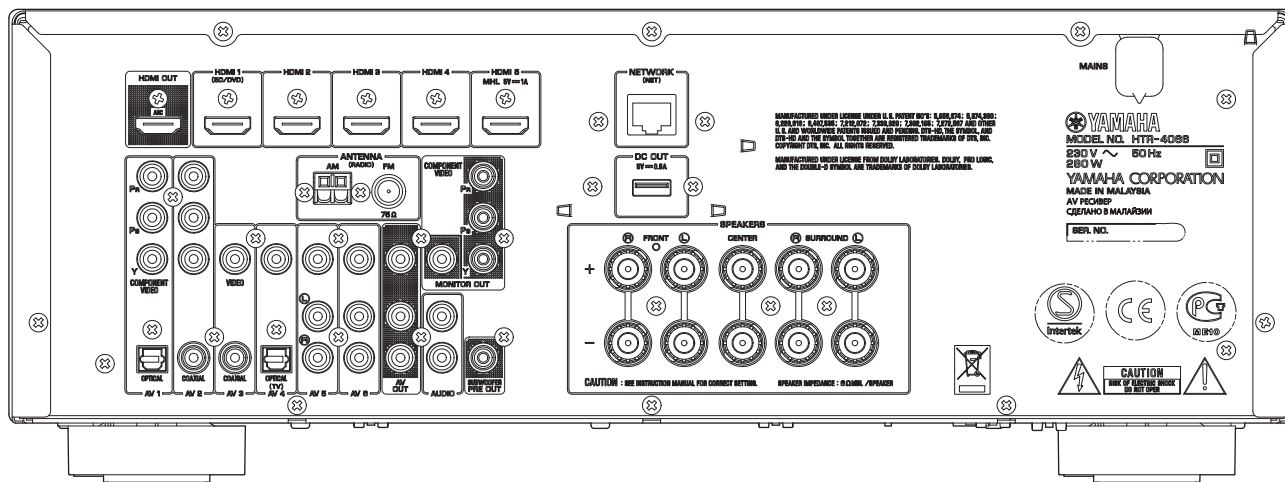


RX-V475/HTR-4066/
RX-V500D

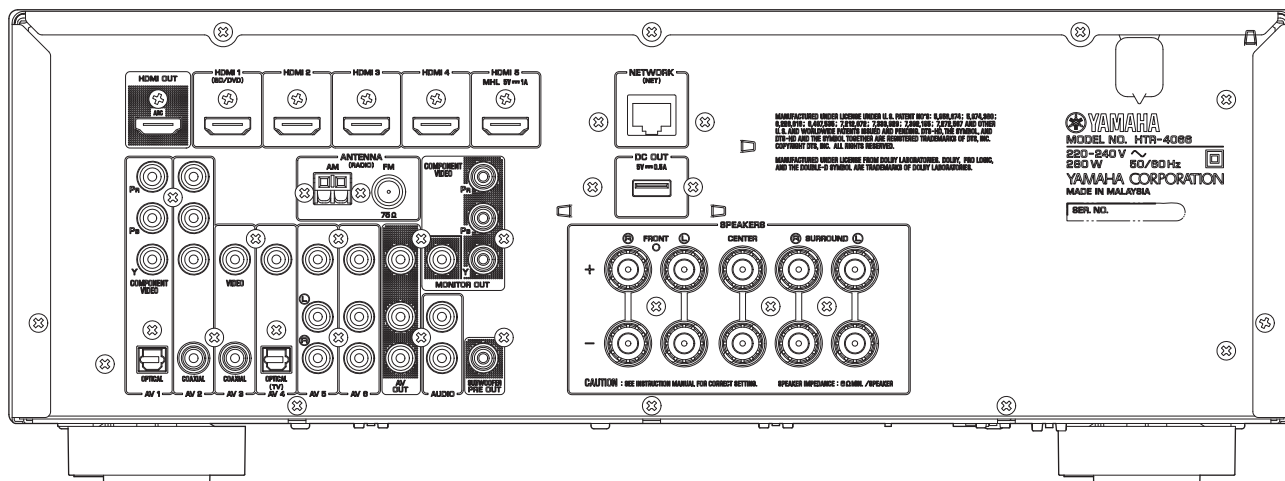
HTR-4066 (A model)



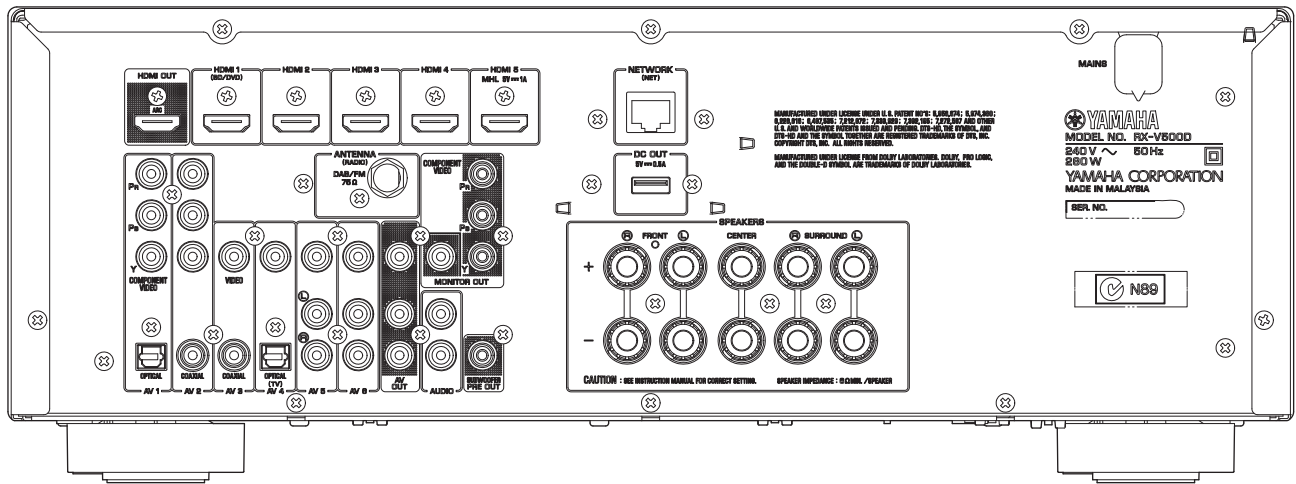
HTR-4066 (B, G, F models)



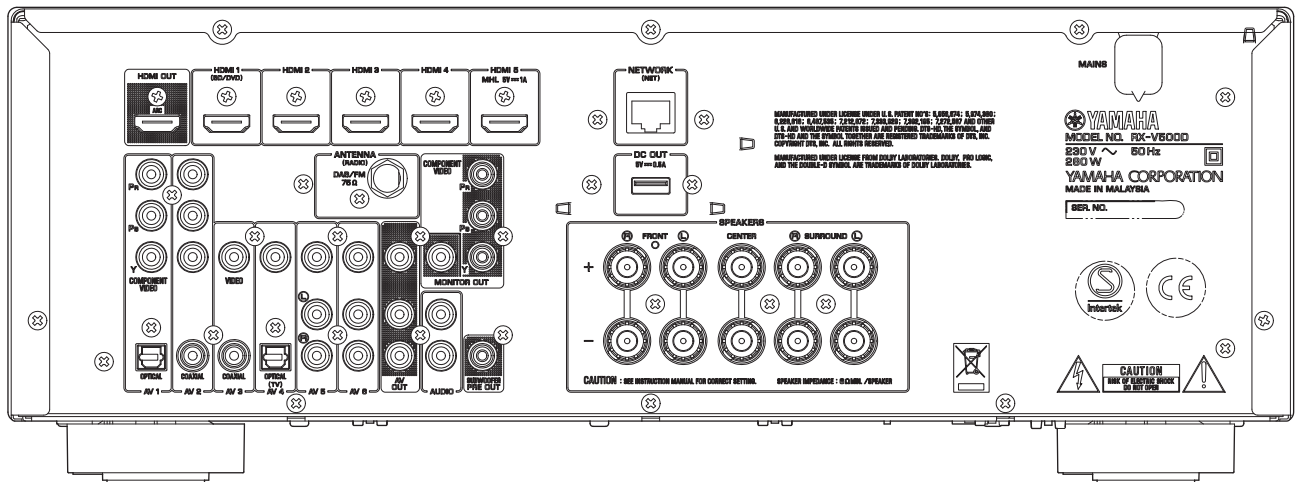
HTR-4066 (L model)



RX-V500D (A model)



RX-V500D (B, G models)



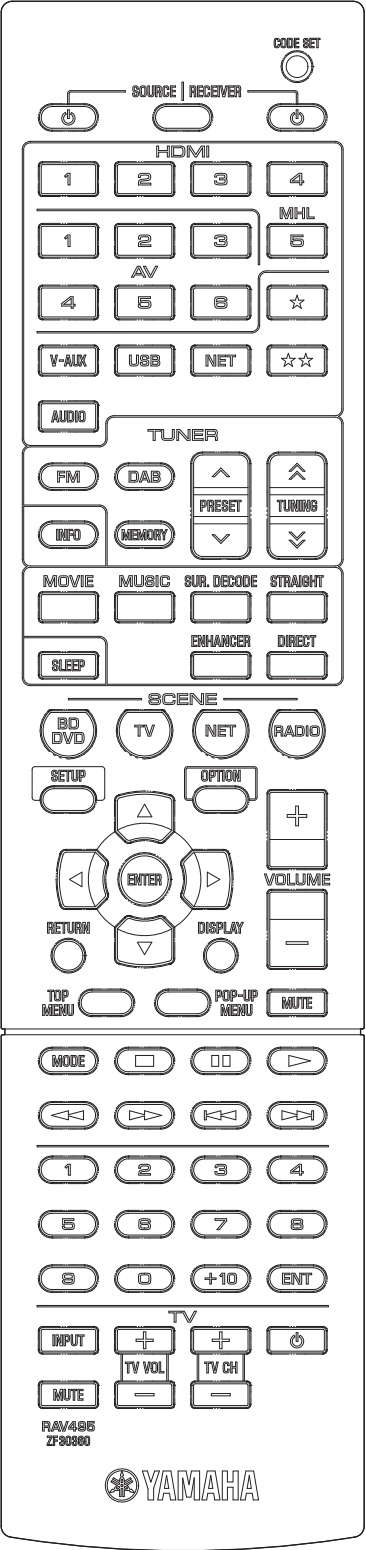
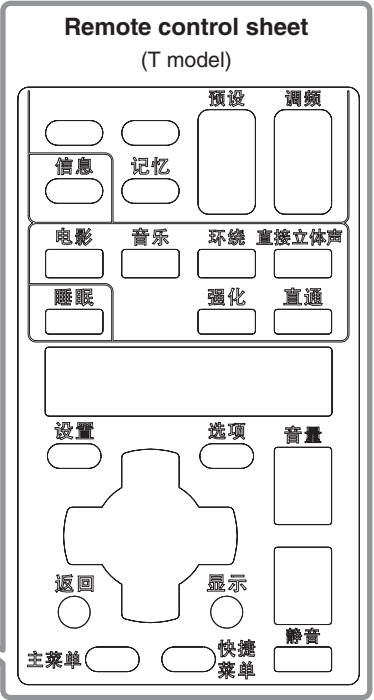
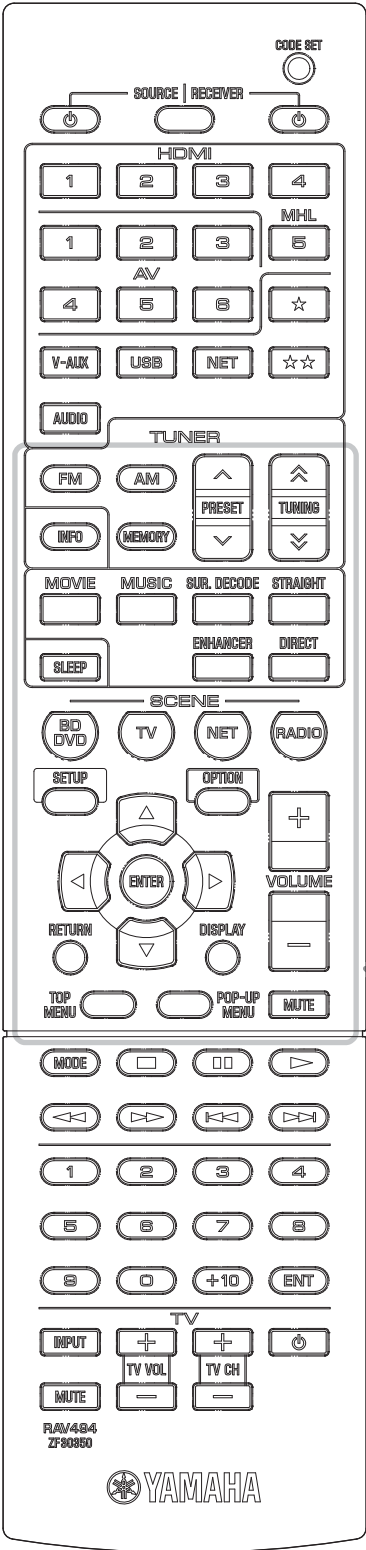
REMOTE CONTROL PANELS

RAV494

RX-V475 / HTR-4066

RAV495

RX-V500D



RX-V475/HTR-4066/
RX-V500D

■ SPECIFICATIONS / 参考仕様

■ Audio Section / オーディオ部

Rated Output Power (Power Amp. Section) /

定格出力 (パワーアンプ部)

(1 kHz, 0.9 % THD)

– 1 channel driven –

U, C models (8 ohms)

FRONT L/R	115 W/ch
CENTER	115 W
SURROUND L/R	115 W/ch

R, T, K, A, B, G, F, L, S, H, J models (6 ohms)

FRONT L/R	115 W/ch
CENTER	115 W
SURROUND L/R	115 W/ch

– 2 channels driven simultaneously –

U, C models (8 ohms)

FRONT L/R	95 W + 95 W
CENTER	95 W
SURROUND L/R	95 W + 95 W

(20 Hz to 20 kHz, 0.09 % THD)

– 2 channels driven simultaneously –

U, C models (8 ohms)

FRONT L/R	80 W + 80 W
R, T, K, A, B, G, F, L, S, H, J models (6 ohms)	
FRONT L/R	80 W + 80 W

Maximum Effective Output Power / 実用最大出力 (JEITA)

(1 kHz, 10 % THD, 6 ohms / 1 channel driven)

[R, T, K, L, S, H, J models]

FRONT L/R	135 W/ch
CENTER	135 W
SURROUND L/R	135 W/ch

Dynamic Power Per Channel / ダイナミックパワー (IHF)

FRONT L/R (1 channel driven)

U, C models

(8 / 6 / 4 / 2 ohms) 110 / 130 / 160 / 180 W

R, T, K, A, B, G, F, L, S, H, J models

(6 / 4 / 2 ohms) 110 / 130 / 160 W

Dynamic Headroom [U, C models]

8 ohms 0.2 dB

Damping Factor / ダンピングファクタ (20 Hz to 20 kHz, 8 ohms)

FRONT L/R to SPEAKER-A 120 or more

Input Sensitivity/Input Impedance / 入力感度／入力インピーダンス

(1 kHz, 100 W/8 ohms)

AV5 etc. 200 mV / 47 k-ohms

Maximum Input Signal / 最大許容入力 (1 kHz, 0.5 % THD)

AV5 etc. (EFFECT ON) 2.3 V

Output Level/Output Impedance / 出力電圧／出力インピーダンス

AV OUT 200 mV / 1.2 k-ohms

SUBWOOFER (2 ch stereo and FRONT SP: small)

1 V / 1.2 k-ohms

Headphone Jack Rated Output/Output Impedance /

ヘッドホン出力／出力インピーダンス (1 kHz, 50 mV, 8 ohms)

AV5 etc. input 100 mV / 470 ohms

Frequency Response / 再生周波数帯域 (10 Hz to 100 kHz)

AV5 etc., FRONT 0 / -3 dB

Signal to Noise Ratio / 信号対雑音比 (IHF-A network)

AV5, etc. (PURE DIRECT) to SP OUT (Input shorted 250 mV)

100 dB or more

Residual Noise / 残留ノイズ (IHF-A network)

FRONT L/R to SP OUT 150 μ V or less

Channel Separation / チャンネルセパレーション

AV5, etc. (Input 5.1 k-ohms shorted)

1 kHz / 10 kHz 60 dB or more / 45 dB or more

Volume Control/Step / 音量可変範囲／ステップ

MUTE / -80 dB to +16.5 dB / 0.5 dB step

Tone Control Characteristics / トーンコントロール特性

FRONT L/R

Bass

Boost/Cut $\pm$ 6 dB / 0.5 dB step, at 50 Hz

Turnover frequency 350 Hz

Treble

Boost/Cut $\pm$ 6 dB / 0.5 dB step, at 20 kHz

Turnover frequency 3.5 kHz

Filter Characteristics / フィルタ特性

FRONT, CENTER, SURROUND small (H.P.F.)

fc=40/60/80/90/100/110/120/160/200 Hz, 12 dB/oct.

SUBWOOFER small (L.P.F.)

fc=40/60/80/90/100/110/120/160/200 Hz, 24 dB/oct.

Optical Jack, Coaxial Jack Support Frequencies /

Optical 端子、Coaxial 端子 対応 fs

32 kHz to 96 kHz

■ Video Section / ビデオ部

Video Signal Type / ビデオ信号方式

U, C, R, K, S, J models NTSC

T, A, B, G, F, L, H models PAL

Composite Video Signal Level / コンポジットビデオ信号

1 Vp-p / 75 ohms

Component Video Signal Level / コンポーネントビデオ信号

Y 1 Vp-p / 75 ohms

Pb/Pr 0.7 Vp-p / 75 ohms

Video Maximum Input Level / ビデオ最大許容入力

(VIDEO Conversion Off)

1.5 Vp-p or more

Video Signal to Noise Ratio / ビデオ信号対雑音比

50 dB or more

Monitor Out Frequency Response / モニター出力周波数帯域

(VIDEO Conversion Off)

Component video signal level / コンポーネントビデオ信号

5 Hz to 60 MHz, -3 dB

■ FM Tuner Section / FM チューナー部

Tuning Range / 受信周波数範囲

U, C models	87.5 MHz to 107.9 MHz
R, L, S, H models	87.5 MHz to 108.0 MHz / 87.50 MHz to 108.00 MHz
T, K, A, B, G, F models	87.50 MHz to 108.00 MHz
J model	76.0 MHz to 90.0 MHz

50 dB Quieting Sensitivity / 50 dB SN 感度 (IHF)

(1 kHz, 100 % MOD.)

Mono	3 µV (20.8 dBf)
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Signal to Noise Ratio / 信号対雑音比 (IHF)

Mono	71 dB
Stereo	69 dB

Harmonic Distortion / 歪率 (1 kHz)

Mono	0.3 %
Stereo	0.5 %

Antenna Input / アンテナ入力

	75 ohms unbalanced
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■ AM Tuner Section / AM チューナー部

Tuning Range / 受信周波数範囲

U, C models	530 to 1,710 kHz
R, L, S, H models	530 to 1,710 kHz / 531 to 1,611 kHz
T, K, A, B, G, F, J models	531 to 1,611 kHz

Antenna / アンテナ

	Loop antenna
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■ DAB Tuner Section [RX-V500D]

Tuning Range

	174 to 240 MHz (Band III)
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Support Audio Format

	MPEG 1 Layer II / MPEG 4 HE AAC v2 (AAC+)
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Antenna

	75 ohms unbalanced
--	--------------------

■ General / 総合

Power Supply / 電源電圧

U, C models	AC 120 V, 60 Hz
R, S models	AC 110–120/220–240 V, 50/60 Hz
T model	AC 220 V, 50 Hz
K model	AC 220 V, 60 Hz
A model	AC 240 V, 50 Hz
B, G, F models	AC 230 V, 50 Hz
L, H models	AC 220–240 V, 50/60 Hz
J model	AC 100 V, 50/60 Hz

Power Consumption / 消費電力

U, C models	270 W / 320 VA
R, T, K, A, B, G, F, L, S, H models	280 W
J model	175 W

Standby Power Consumption (reference data) /

待機時消費電力 (参考値)

HDMI control: OFF / Standby through: OFF	0.1 W or less
HDMI control: ON / Standby through: ON	
INPUT: HDMI1 (HDMI no signal)	1.0 W (typical)
Network standby: ON	2.0 W (typical)

Maximum Power Consumption [R, S models]

	600 W
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Dimensions (W x H x D) / 寸法 (幅 × 高さ × 奥行き)

	435 x 161 x 315 mm (17-1/8" x 6-3/8" x 12-3/8")
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Weight / 質量

	8.1 kg (17.9 lbs.)
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Finish / 仕上げ

[RX-V475]	
T model	Gold color
U, C, R, T, K, A, B, G, F, L, S, H, J models	Black color
R, K, A, B, G, F, L models	Titanium color
[HTR-4066]	
T model	Gold color
U, R, T, K, A, B, G, F, L models	Black color
K, A, B, G models	Titanium color
[RX-V500D]	
A, B, G models	Black color
A, B, G models	Titanium color

Accessories / 付属品

Remote control	x 1
Battery (R03, AAA, UM-4)	x 2
FM antenna (1.4 m) (RX-V475/HTR-4066)	x 1
AM antenna (1 m) (RX-V475/HTR-4066)	x 1
DAB/FM antenna (1.6 m) (RX-V500D)	x 1
YPAO microphone (6 m)	x 1
Remote control sheet (T model)	x 1
Antenna isolator (T model)	x 1
Conversion plug (T model)	x 1

* Specifications are subject to change without notice.

※ 参考仕様および外観は、製品の改良のため予告なく変更することがあります。

U	U.S.A. model	G	European model
C	Canadian model	F	Russian model
R	General model	L	Singapore model
T	Chinese model	S	Brazilian model
K	Korean model	H	Thai model
A	Australian model	J	Japanese model
B	British model		



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Fraunhofer Institut
Integrierte Schaltungen

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This receiver supports network connections.

本機はネットワーク接続に対応しています。



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Digital Audio Broadcasting



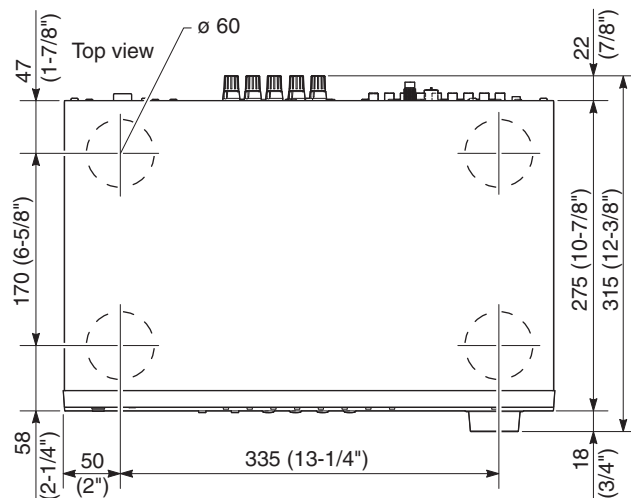
Digital Audio Broadcasting

The unit supports DAB/DAB+ tuning.

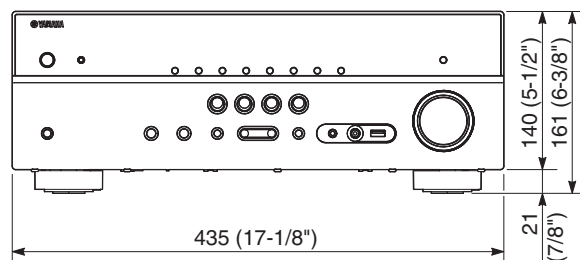


AAC ロゴマーク はドルビーラボラトリーズの商標です。

• DIMENSIONS



Front view



Unit: mm (inch)
単位: mm (インチ)

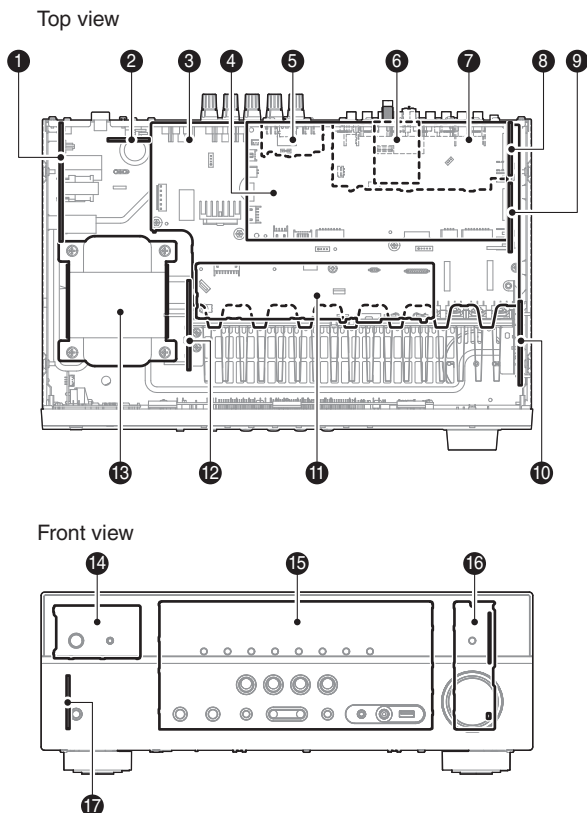
• SET MENU TABLE

MAIN MENU	SUB-MENU	PARAMETER			VALUE [INITIAL VALUE]	
Speaker	Configuration	Subwoofer			[Use] / None	
		Front			[Small] / Large	
		Center			[Small] / Large / None	
		Surround			[Small] / Large / None	
		Crossover			40 Hz / 60 Hz / [80 Hz] / 90 Hz / 100Hz / 110 Hz / 120 Hz / 160 Hz / 200 Hz	
		Subwoofer Phase			[Normal] / Reverse	
		Extra Bass			[Off] / On * “Extra Bass” is not available when “Subwoofer” is set to “None”, or when “Front” is set to “Small”. “Extra Bass” は “Subwoofer : None” または “Front : Small” と設定した場合、選択不可能	
	Distance	Unit			Meter / Feet	
		Front L			0.30 to 24.00 m, [3.00 m], 0.05 m step	
		Front R			1.0 to 80.0 ft, [10.0 ft], 0.2 ft step	
		Center			0.30 to 24.00 m, [2.60 m], 0.05 m step 1.0 to 80.0 ft, [8.6 ft], 0.2 ft step	
		Surround L			0.30 to 24.00 m, [2.40 m], 0.05 m step	
		Surround R			1.0 to 80.0 ft, [8.0 ft], 0.2 ft step	
		Subwoofer			0.30 to 24.00 m, [3.00 m], 0.05 m step 1.0 to 80.0 ft, [10.0 ft], 0.2 ft step	
	Level	Front L			-10.0 to +10.0 dB, [0.0 dB], 0.5 dB step	
		Front R				
		Center			-10.0 to +10.0 dB, [-1.0 dB], 0.5 dB step	
		Surround L				
		Surround R			-10.0 to +10.0 dB, [0.0 dB], 0.5 dB step	
		Subwoofer				
	Equalizer	EQ Select			PEQ / [GEQ] / Off * “PEQ” is available only when the YPAO has been performed. “PEQ”は自動測定（YPAO）実行後のみ選択可能	
		GEQ Edit	Front L	63 Hz		-6.0 to +6.0 dB, [0 dB], 0.5 dB step
			Front R	160 Hz		
			Center	400 Hz		
			Surround L	1 kHz		
			Surround R	2.5 kHz		
				6.3 kHz		
				16 kHz		
		Test Tone				[Off] / On

MAIN MENU	SUB-MENU	PARAMETER	VALUE [INITIAL VALUE]
HDMI	Configuration	HDMI Control	[Off] / On (U, C, R, T, K, A, B, G, F, L, S, H models) Off / [On] (J model)
		Audio Output	
		Amp	Off / [On]
		HDMI OUT (TV)	[Off] / On
		* This setting is available only when "HDMI Control" is set to "Off". "HDMI Control" が "Off" の場合のみ設定可能	
		Standby Through	[Off] / On * This setting is available only when "HDMI Control" is set to "Off". "HDMI Control" が "Off" の場合のみ設定可能
		TV Audio Input	AV1 / AV2 / AV3 / [AV4] / AV5 / AV6 / AUDIO * This setting is available only when "HDMI Control" is set to "On". "HDMI Control" が "On" の場合のみ設定可能
		Standby Sync	Off / On / [Auto] * This setting is available only when "HDMI Control" is set to "On". "HDMI Control" が "On" の場合のみ設定可能
		ARC	Off / [On] * This setting is available only when "HDMI Control" is set to "On". "HDMI Control" が "On" の場合のみ設定可能
		SCENE	
		BD / DVD	Off / [On]
		TV	
		NET	[Off] / On
		RADIO	
		* This setting is available only when "HDMI Control" is set to "On". "HDMI Control" が "On" の場合のみ設定可能	
Sound	DSP Parameter	CINEMA DSP 3D Mode	Off / [On]
		Panorama	[Off] / On
		Center Width	0 to 7, [3]
		Dimension	-3 to +3, [0]
		Center Image	0.0 to 1.0, [0.3]
	Lipsync	Select	Manual / [Auto]
		Adjustment	0 to 250 ms, [0 ms], 1 ms step
	Volume	Dynamic Range	[Maximum] / Standard / Min/Auto
		Max Volume	-30.0 to +15.0 dB / +16.5 dB (Maximum volume), [+16.5 dB], 5.0 dB step
		Initial Volume	[Off] / Mute / -80.0 to +16.5 dB, 0.5 dB step
ECO	Auto Power Standby	Power Mode	U, C, R, T, K, A, L, S, H, J models: [Off] / 2 hours / 4 hours / 8 hours / 12 hours B, G, F models: Off / 2 Hours / 4 Hours / [8 Hours] / 12 Hours
	ECO Mode		[Off] / On

MAIN MENU	SUB-MENU	PARAMETER	VALUE [INITIAL VALUE]
Function	Input Rename		Input sources: HDMI1 / HDMI2 / HDMI3 / HDMI4 / HDMI5 / AV1 / AV2 / AV3 / AV4 / AV5 / AV6 / AUDIO / USB / V-AUX Input is possible to 9 characters Input possible Character type Capital: A to Z Small: a to z Figure: 0 to 9 Symbols: / () = + , - etc. Space Preset name select: Blu-ray / DVD / SetTopBox / Game / TV / DVR / CD / CD-R / Satellite / VCR / Tape / MD / PC / iPod / HD DVD
Function	Dimmer		-4 to 0 (higher to brighten), [0]
	Memory Guard		[Off] / On
	DC OUT	Power Mode	[Continuous] / Power Sync.
Network	Information	Status	Disconnect / Connect (status of the NETWORK jack)
		MAC Address	xx:xx:xx:xx:xx:xx
		IP Address	xxx.xxx.xxx. x
		Subnet Mask	xxx.xxx.xxx. x
		Default Gateway	xxx.xxx.xxx. x
		DNS Server (Primary)	xxx.xxx.xxx. x
		(Secondary)	xxx.xxx.xxx. x
		vTuner (Internet radio) ID	xxxxxxxxxxx
	IP Address	DHCP	Off / [On]
		* The following setting is available only when "DHCP" is set to "Off". 以下は "DHCP" が "Off" の場合のみ設定可能	
		IP Address	xxx.xxx.xxx. x
		Subnet Mask	xxx.xxx.xxx. x
		Default Gateway	xxx.xxx.xxx. x
		DNS Server (Primary)	xxx.xxx.xxx. x
		(Secondary)	xxx.xxx.xxx. x
Network	MAC Address Filter		[Off] / On
		MAC Address 1-10	xx:xx:xx:xx:xx:xx * This setting is available only when "MAC Address Filter" is set to "On". "MAC Address Filter" が "On" の場合のみ設定可能
		DMC Control	Disable / [Enable]
		Network Standby	[Off] / On
		Network Name	Input is possible to 15 characters
	Network Update	Perform Update	
		Firmware Version	x.xx
		System ID	xxxxxxxx
Language			English (English) / 日本語 (Japanese) / Français (French) / Deutsch (German) / Español (Spanish) / Русский (Russian) / Italiano (Italian) / 中文 (Chinese)
(U, C, R, T, K, A, B, G, F, L, S, H models)			

INTERNAL VIEW



- ① OPERATION (2) P.C.B.
- ② MAIN (4) P.C.B. (R, S models)
- ③ MAIN (1) P.C.B.
- ④ DIGITAL P.C.B.
- ⑤ OPERATION (8) P.C.B.
- ⑥ AM/FM TUNER (RX-V475/HTR-4066)
DAB P.C.B. (RX-V500D)
- ⑦ OPERATION (3) P.C.B.
- ⑧ MAIN (3) P.C.B.
- ⑨ MAIN (2) P.C.B.
- ⑩ MAIN (5) P.C.B.
- ⑪ OPERATION (4) P.C.B.
- ⑫ OPERATION (9) P.C.B.
- ⑬ POWER TRANSFORMER
- ⑭ OPERATION (5) P.C.B.
- ⑮ OPERATION (1) P.C.B.
- ⑯ OPERATION (6) P.C.B.
- ⑰ OPERATION (7) P.C.B.

SERVICE PRECAUTIONS / サービス時の注意事項

Safety measures

- Some internal parts in this product contain high voltages and are dangerous.
Be sure to take safety measures during servicing, such as wearing insulating gloves.
- Note that the capacitors indicated below are dangerous even after the power is turned off because an electric charge remains and a high voltage continues to exist there.
Before starting any repair work, connect a discharging resistor (5 k-ohms/10 W) to the terminals of each capacitor indicated below to discharge electricity.
The time required for discharging is about 30 seconds per each.

C2084 and C2085 on MAIN (1) P.C.B.

C5407 on OPERATION (2) P.C.B.

For details, refer to "PRINTED CIRCUIT BOARDS".

安全対策

- この製品の内部には高電圧部分があり危険です。修理の際は、絶縁性の手袋を使用するなどの安全対策を行ってください。
- 下記のコンデンサには電源を OFF にした後も電荷が残り、高電圧が維持されており危険です。
修理作業前に放電用抵抗 (5 k Ω /10 W) を下記の各コンデンサの端子間に接続して放電してください。
放電所用時間は各々約 30 秒間です。

MAIN (1) P.C.B. の C2084、C2085

OPERATION (2) P.C.B. の C5407

詳しくは "PRINTED CIRCUIT BOARDS" を参照してください。

■ DISASSEMBLY PROCEDURES / 分解手順

(Remove parts in the order as numbered.)

Disconnect the power cable from the AC outlet.

(番号順に部品を外してください。)

AC 電源コンセントから、電源コードを抜いてください。

1. Removal of Top Cover

- Remove 4 screws (①) and 5 screws (②). (Fig. 1)
- Lift the rear of the top cover to remove it. (Fig. 1)

1. トップカバーの外し方

- ① のネジ 4 本、② のネジ 5 本を外します。(Fig. 1)
- トップカバーの後部を持ち上げ、外します。(Fig. 1)

2. Removal of Front Panel Unit

- Remove 7 screws (③), and remove W4501 and W4761. (Fig. 1)
- Remove CB21, CB61, CB371, CB477 and CB952. (Fig. 1)
- Unlock and remove CB525. (Fig. 1)
- Release 2 hooks on both ends and remove the front panel unit. (Fig. 1)

2. フロントパネルユニットの外し方

- ③ のネジ 7 本を外し、W4501、W4761 を外します。(Fig. 1)
- CB21、CB61、CB371、CB477、CB952 を外します。(Fig. 1)
- ロックを外し、CB525 を外します。(Fig. 1)
- フック 2 箇所を外し、フロントパネルユニットを外します。(Fig. 1)

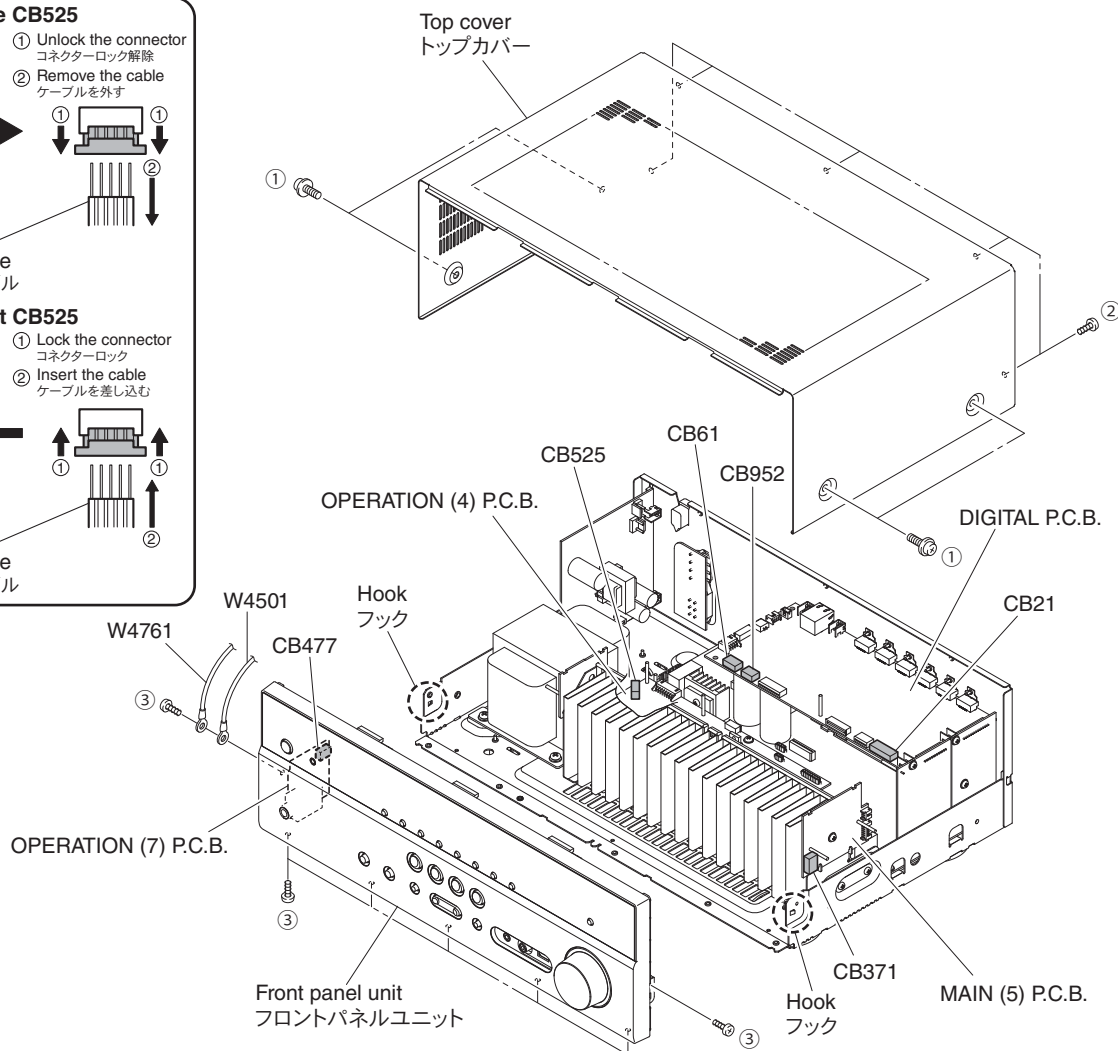
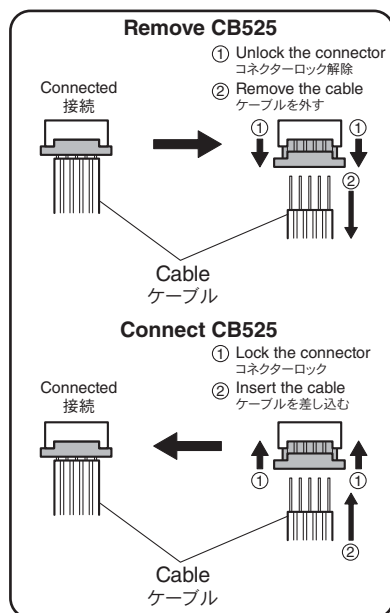


Fig. 1

3. Removal of DIGITAL P.C.B.

- Remove 2 screws (④) and 6 screws (⑤). (Fig. 3)
- Remove 2 screws (⑥). (Fig. 2)
- Remove CB22, CB26, CB64, CB65 and CB91. (Fig. 2)
- Unlock and remove CB24 and CB25. (Fig. 2)
- Remove the DIGITAL P.C.B. which is connected directly to the MAIN (2) P.C.B. and MAIN (3) P.C.B. with board-to-board connectors. (Fig. 2)

4. Removal of AMP Unit

- Remove 4 screws (⑦), 4 screws (⑧) and 2 screws (⑨). (Fig. 2)
- Remove 3 screws (⑩). (Fig. 3)
- Remove the amp unit. (Fig. 2)

3. DIGITAL P.C.B. の外し方

- ④ のネジ 2 本、⑤ のネジ 6 本を外します。(Fig. 3)
- ⑥ のネジ 2 本を外します。(Fig. 2)
- CB22、CB26、CB64、CB65、CB91 を外します。(Fig. 2)
- ロックを外し、CB24、CB25 を外します。(Fig. 2)
- DIGITAL P.C.B. を外します。ただし、DIGITAL P.C.B. は MAIN (2) P.C.B.、MAIN (3) P.C.B. に基板対基板コネクタで直接接続されています。(Fig. 2)

4. アンプユニットの外し方

- ⑦ のネジ 4 本、⑧ のネジ 4 本、⑨ のネジ 2 本を外します。(Fig. 2)
- ⑩ のネジ 3 本を外します。(Fig. 3)
- アンプユニットを外します。(Fig. 2)

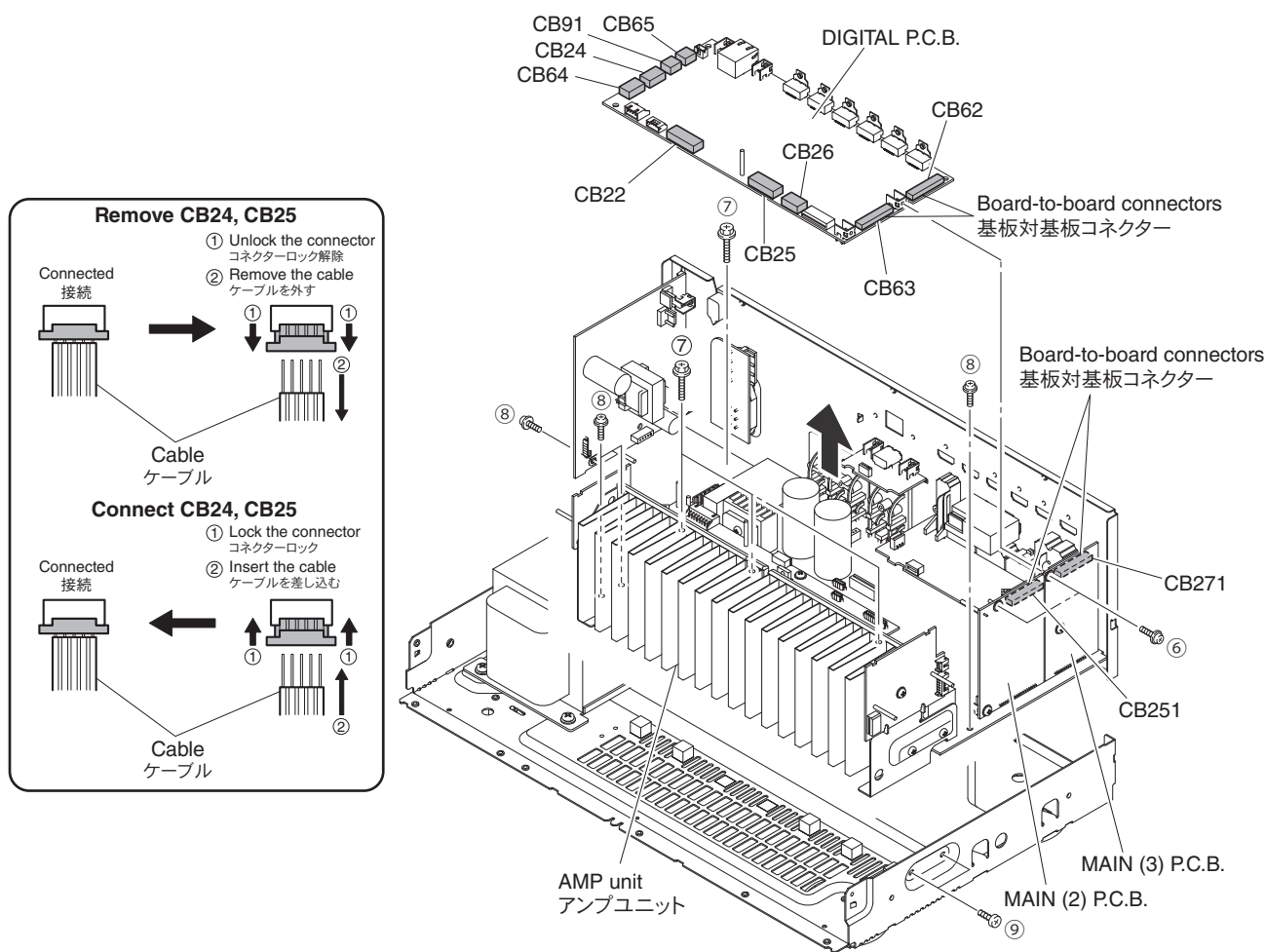


Fig. 2

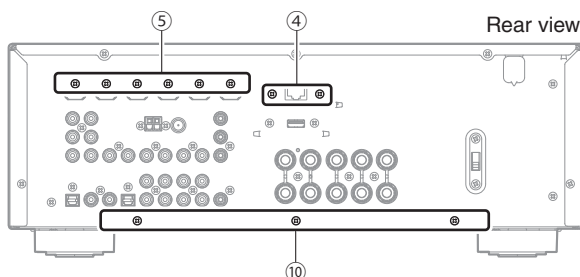


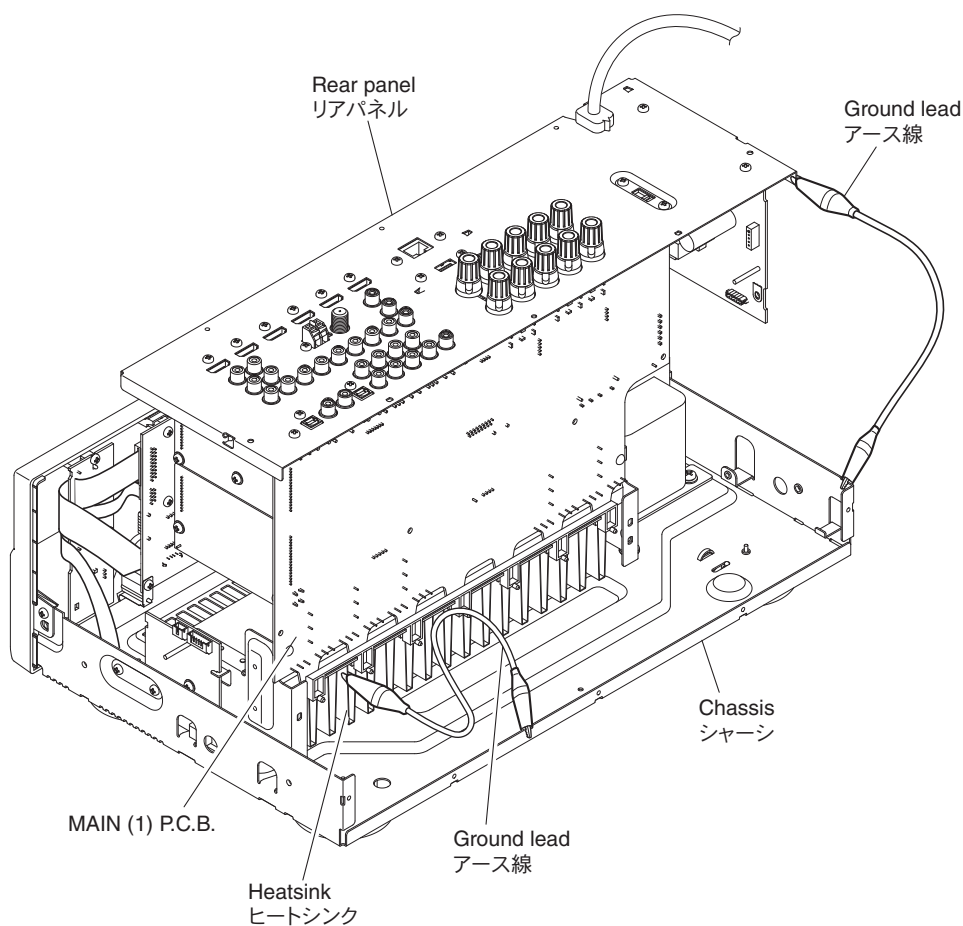
Fig. 3

When checking the MAIN (1) P.C.B.:

- Place the P.C.B.s (with rear panel) upright. (Fig. 4)
- Connect the heatsink and rear panel to the chassis with a ground lead or the like. (Fig. 4)
- Reconnect all cables (connectors) that have been disconnected.
- When connecting the flexible flat cable, be careful with polarity.

MAIN (1) P.C.B. をチェックする場合には：

- リアパネルと一緒に P.C.B. を立ち上げて置きます。(Fig. 4)
- ヒートシンク、リアパネルをリード線等でシャーシに接続してください。(Fig. 4)
- 外したケーブル（コネクター）をすべて接続します。
- フラットケーブルを接続する際、極性に注意してください。

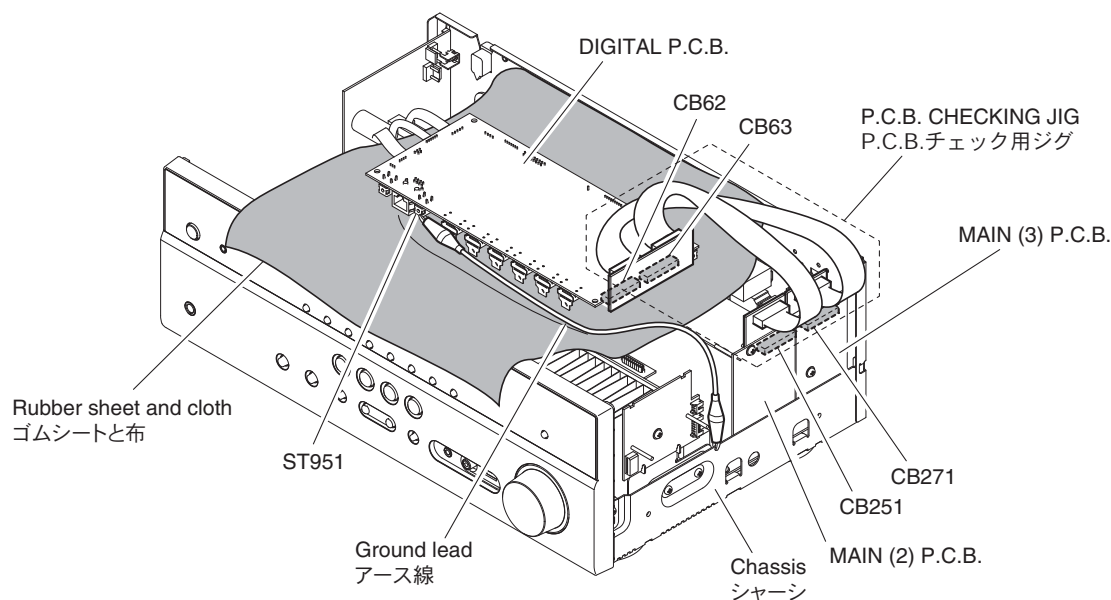
**Fig. 4**

When checking the DIGITAL P.C.B.:

- Put the rubber sheet and cloth over this unit, and place the DIGITAL P.C.B. on them. (Fig. 5)
- Connect ST951 on DIGITAL P.C.B. to the chassis with a ground lead. (Fig. 5)
- Reconnect all cables (connectors) that have been disconnected. Be sure to use the P.C.B. CHECKING JIG (Part No. ZG780000) to connect between the following connectors.
 CB62 on DIGITAL P.C.B. – CB271 on MAIN (3) P.C.B.
 CB63 on DIGITAL P.C.B. – CB251 on MAIN (2) P.C.B.
- When connecting the flexible flat cable, be careful with polarity.

DIGITAL P.C.B. をチェックする場合には：

- 本機の上にゴムシートと布を敷き、その上に DIGITAL P.C.B. を置きます。(Fig. 5)
- DIGITAL P.C.B. の ST951 のアースをリード線でシャーシに接続してください。(Fig. 5)
- 外したケーブル（コネクター）をすべて接続します。ただし下記のコネクター間を接続するには P.C.B. チェック用ジグ（部品番号：ZG780000）を使用してください。
 DIGITAL P.C.B.のCB62 – MAIN (3) P.C.B.のCB271
 DIGITAL P.C.B.のCB63 – MAIN (2) P.C.B.のCB251
- フラットケーブルを接続する際、極性に注意してください。

**Fig. 5**

■ UPDATING FIRMWARE / ファームウェアのアップデート

When the following parts are replaced, the firmware must be updated to the latest version.

DIGITAL P.C.B.
IC2 on DIGITAL P.C.B.
IC43 on DIGITAL P.C.B.
IC953 on DIGITAL P.C.B.

下記の部品を交換した場合、ファームウェアを最新バージョンにアップデートする必要があります。

DIGITAL P.C.B.
DIGITAL P.C.B. の IC2
DIGITAL P.C.B. の IC43
DIGITAL P.C.B. の IC953

● Confirmation of firmware version

Before and after updating the firmware, check the firmware version by using the self-diagnostic function menu.

Start up the self-diagnostic function and select "S4. ROM VERSION/CHECKSUM" menu.

Using the sub-menu, have the firmware version displayed, and note them down.

(For details, refer to "SELF-DIAGNOSTIC FUNCTION")

- * When the firmware version is different from written one after updating, perform the updating procedure again from the beginning.

● Initializing the back-up IC (EEPROM: IC22 on DIGITAL P.C.B.)

After updating the firmware, the back-up IC MUST be initialized by the following procedure store the setting information (soundfield parameters, system memory and tuner presetting, etc.) properly.

Start up the self-diagnostic function and select "S3. FACTORY PRESET" menu.

(For details, refer to "SELF-DIAGNOSTIC FUNCTION")

Select "PRESET RSRV", press the "⏻" (Power) key to turn off the power once and turn on the power again. Then the back-up IC is initialized.

● Required Tools

- USB storage device
- Firmware
RX-V475/HTR-4066: R0326-xxxx.bin
RX-V500D: R0330-xxxx.bin

● Preparation

1. Download the latest firmware from the specified download source to the folder of the PC.
2. Copy the latest firmware from the PC to the root folder of the USB storage device.

Note: When the latest firmware is copied to a sub-folder of the USB storage device, the update will not proceed.

● ファームウェアのバージョンの確認

ファームウェアのアップデートの前後に、ファームウェアのバージョンをダイアグで確認します。

ダイアグを起動し、"S4. ROM VERSION/CHECKSUM" メニューを選択します。

サブメニューでファームウェアのバージョンを表示し、それらを書きとめます。

(詳細は "ダイアグ" を参照してください。)

- ※ アップデート後、ファームウェアのバージョンが書き込まれたものと異なる場合、アップデートの操作を最初からやり直してください。

● バックアップ IC の初期化 (EEPROM : DIGITAL P.C.B. の IC22)

ファームウェアのアップデート後、設定情報（音場プログラムのパラメーターやシステムメモリー、チューナープリセット等）を正常に保存するために、下記の方法でバックアップ IC を初期化する必要があります。

本機のダイアグを起動し、"S3. FACTORY PRESET" メニューを選択します。

(詳細は "ダイアグ" を参照してください。)

"PRESET RSRV" を選択し、"⏻"（電源）キーを押して電源を一度きってから、もう一度電源を入れるとバックアップ IC が初期化されます。

● 必要なツール

- USB フラッシュメモリー
- ファームウェア
RX-V475 : R0326-xxxx.bin

● 準備

1. 指定のダウンロード先から、最新のファームウェアを PC のフォルダへダウンロードしてください。
2. PC から USB フラッシュメモリーのルートフォルダへ最新のファームウェアをコピーします。

注意：最新のファームウェアをサブフォルダにコピーした場合、書き込みはできません。

● Operation Procedures

1. Insert the USB storage device to the USB jack. (Fig. 1)
2. While pressing the "INFO" key, connect the power cable to the AC outlet. (Fig. 1)

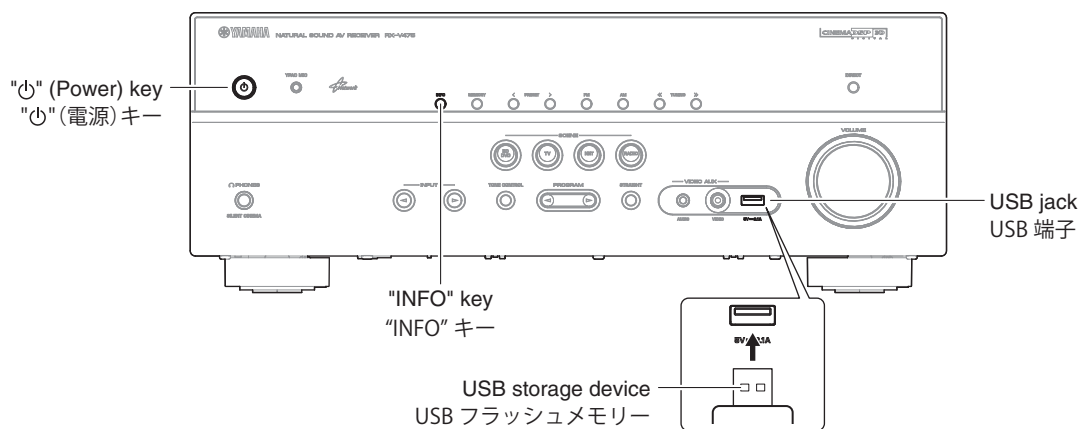


Fig. 1

● 操作手順

1. USB 端子に USB フラッシュメモリーを差し込みます。(Fig. 1)
2. "INFO" キーを押しながら、電源コードを AC コンセントに接続します。(Fig. 1)

3. The USB UPDATE mode is activated and "USB UPDATE" is displayed. Writing of the firmware starts automatically. (Fig. 2)

Writing is started. / 書き込み開始

USB UPDATE



VERIFYING..



Sx-xxxx%

Writing being executed. / 書き込み中

Fig. 2

3. USB UPDATE モードが起動し、"USB UPDATE" が表示されて、ファームウェアの書き込みが自動的に開始されます。(Fig. 2)

4. When writing of the firmware is completed, "UPDATE SUCCESS", "PLEASE..." and "POWER OFF!" are displayed repeatedly. (Fig. 3)

Writing is completed. / 書き込み完了



Fig. 3

4. ファームウェアの書き込み完了後、"UPDATE SUCCESS"、"PLEASE..."、"POWER OFF!" が繰り返し表示されます。(Fig. 3)

5. Press the "Power" key to turn off the power. (Fig. 1)
6. Remove the USB storage device from the USB jack. (Fig. 1)
7. Start up the self-diagnostic function and check that the firmware version is the same as written one. (For details, refer to "Confirmation of firmware version")

5. "Power" (電源) キーを押して電源を切ります。(Fig. 1)
6. USB 端子から USB フラッシュメモリーを抜きます。(Fig. 1)
7. ダイアグを起動し、ファームウェアのバージョンが、書き込まれたものと同じであることを確認します。
(詳細は "ファームウェアのバージョンの確認" を参照してください。)

■ SELF-DIAGNOSTIC FUNCTION / ダイアグ（自己診断機能）

This unit has self-diagnostic functions that are intended for inspection, measurement and location of faulty point.

There are 27 main menu items, each of which has sub-menu items.

Listed in the table below are main menu items and sub-menu items.

Note: Some of the menu items listed below may not apply to the models covered in this service manual.

本機には、検査、測定、不良箇所の発見を目的にしたダイアグ（自己診断機能）があります。

ダイアグには 27 個のメインメニューがあり、そのそれぞれにサブメニューがあります。

下表はダイアグメニュー一覧です。

注意：以下のメニュー項目の一部は、このサービスマニュアルに記載されているモデルに適用されない場合があります。

No.	Main menu	No.	Sub-menu
A: Audio system / オーディオ系			
A1	DSP AUDIO	1	DSP MARGIN
		2	DSP NON MARGIN
		3	DSP FULL CENTER
		4	DSP FULL SURROUND
		5	DSP FULL SURROUND BACK (Not for service / サービスでは使用しません)
		6	DSP FULL SUBWOOFER
A2	DIRECT AUDIO	1	ANALOG DIRECT
		2	NET DIRECT (Not for service / サービスでは使用しません)
A3	HDMI AUDIO	1	HDMI AUTO
		2	ARC
A4	SPEAKERS SET	1	FULL MUTE
		2	BI-AMP (Not for service / サービスでは使用しません)
		3	AC B : HIGH (Not for service / サービスでは使用しません)
		4	AC B : LOW (Not for service / サービスでは使用しません)
A5	MIC CHECK	1	MIC ROUTE CHECK
A6	INVALID ITEM (Not for service / サービスでは使用しません)	1	INVALID ITEM
		2	INVALID ITEM
		3	INVALID ITEM
A7	DIR PLL	1	DIR PLL
A8	MANUAL TEST	1	TEST ALL
H: HDMI / HDMI			
H1	INVALID ITEM (Not for service / サービスでは使用しません)	1	INVALID ITEM
		2	INVALID ITEM
D: Display system / 表示系			
D1	FL CHECK	1	INITIAL DISPLAY
		2	ALL SEGMENT OFF
		3	ALL SEGMENT ON
		4	CHECK PATTERN 1
		5	CHECK PATTERN 2
U: Universal system / 特殊端子系			
U1	USB	1	USB FRONT 1 TRACK
		2	USB BOOT (Not for service / サービスでは使用しません)
		3	USB_VBUS HIGH POWER (Not for service / サービスでは使用しません)
		4	INVALID ITEM
N: Network system / ネットワーク系			
N1	NETWORK	1	IP ADDRESS CHECK
		2	MAC ADDRESS CHECK
		3	LINE NOISE 100 MDI (Not for service / サービスでは使用しません)
		4	LINE NOISE 100 MDIX (Not for service / サービスでは使用しません)
		5	LINE NOISE 10 MDI (Not for service / サービスでは使用しません)
		6	LINE NOISE 10 MDIX (Not for service / サービスでは使用しません)
		7	LINK CHECK
		8	EXT TEST

No.	Main menu	No.	Sub-menu
C: Communication system / 通信・バスライン系			
C1	DIGITAL PCB CHECK	1	ALL
		2	MCPU OSD
		3	OSD HDMI
		4	VIDEO I/F (Not for service / サービスでは使用しません)
		5	BUS DIR
		6	BUS DSP
		7	EEPROM
		8	TUNER
C2	HDMI INFO	1	HDMI MODEL NAME
		2	HDMI PRODUCT ID (Not for service / サービスでは使用しません)
C3	NETWORK IC CHECK	1	ALL
		2	NET RAM
		3	PHY TEST
		4	APL ID
V: Video system / ビデオ系			
V1	ANALOG VIDEO CHECK	1	ANALOG BYPASS
		2	MUTE CHECK
V2	DIGITAL VIDEO CHECK	1	HDMI REPEAT
		2	OSD-VIDEO OUT
R: Radio system / TUNER・衛星放送系			
R1	DAB (RX-V500D model)	1	SIGNAL QUALITY (Not for service / サービスでは使用しません)
		2	DAB MODULE VERSION
P: Power supply and protection system / 電源・プロテクション系			
P1	SYSTEM MONITOR	1	DC
		2	PS
		3	TMP
		4	OUTPUT LEVEL
		5	LIMITER CONTROL
		6	USB-VBUS
		7	KEY
P2	PROTECTION HISTORY	1	1. HISTORY 1
		2	1. POWER PORT
		3	1. LAST INPUT
		4	1. LAST VOLUME
		5	2. HISTORY 2
		6	2. POWER PORT
		7	2. LAST INPUT
		8	2. LAST VOLUME
		9	3. HISTORY 3
		10	3. POWER PORT
		11	3. LAST INPUT
		12	3. LAST VOLUME
		13	4. HISTORY 4
		14	4. POWER PORT
		15	4. LAST INPUT
		16	4. LAST VOLUME
T: Troubleshooting Information / サービス・設計用故障解析情報			
T1	TROUBLE SHOOTING INFORMATION	1	OPERATING TIME
		2	POWER-RELAY ON
		3	POWER AMP B
		4	OUTPUT LEVEL
		5	NRC (Net Restart Counter) (Not for service / サービスでは使用しません)

No.	Main menu	No.	Sub-menu
S: System and version system / システム・バージョン系			
S1	FIRMWARE UPDATE	1	DSP FIRMWARE UPDATE (Not for service / サービスでは使用しません)
S2	SET INFORMATION	1	INITIAL DISPLAY
		2	MODEL/DESTINATION
S3	FACTORY PRESET	1	PRESET INHIBIT
		2	PRESET RESERVED
S4	ROM VERSION/CHECKSUM	1	SYSTEM VERSION
		2	MICROPROCESSOR VERSION
		3	MICROPROCESSOR CHECKSUM
		4	DSP VERSION
		5	DSP CHECKSUM
		6	OSD VERISON
		7	OSD CHECKSUM
		8	NETWORK VERSION
		9	NETWORK CHECKSUM
		10	USB CONTROLLER VERSION (Not for service / サービスでは使用しません)
		11	USB CONTROLLER CHECKSUM (Not for service / サービスでは使用しません)
S5	SOFT SWITCH	1	SWITCH MODE
		2	MODEL NAME
S6	SYSTEM INFORMATION	1	MODEL/DESTINATION
		2	VERIFY (Not for service / サービスでは使用しません)

● Starting Self-Diagnostic Function

While pressing the "TONE CONTROL" and "INFO" keys, press the "⏻" (Power) key to turn on the power, and release those 2 keys.

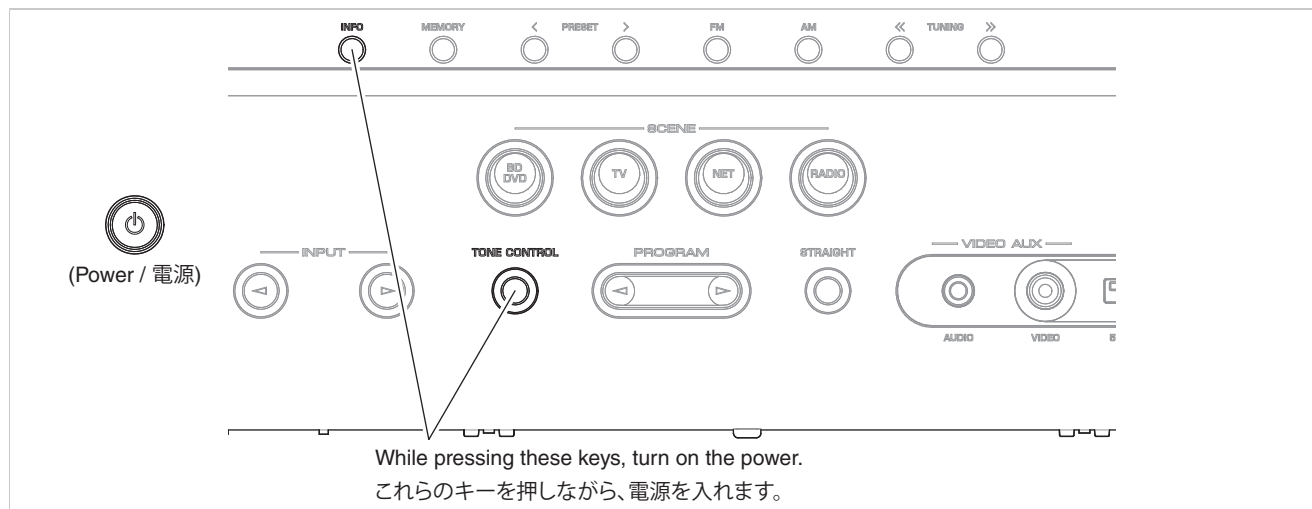
The self-diagnostic function mode is activated.

● ダイアグの起動

"TONE CONTROL" と "INFO" キーを押しながら "⏻" (電源) キーを押して電源を入れた後、2つのキーを放します。

ダイアグが起動します。

Keys of this unit / 本機キー



● Starting Self-Diagnostic Function in the protection cancel mode

If the protection function works and causes hindrance to troubleshooting, cancel the protection function by the procedure below, and it will be possible to enter the self-diagnostic function mode. (The protection functions other than the excess current detect function will be disabled.)

While pressing the "TONE CONTROL" and "INFO" keys, press the "⏻" (Power) key to turn on the power and keep pressing those 2 keys and "⏻" (Power) key for 3 seconds or longer.

The self-diagnostic function mode is activated with the protection functions disabled.

In this mode, the "SLEEP" segment of the FL display flashes to indicate that the mode is self-diagnostic function mode with the protection functions disabled.

● プロテクション解除モードでの起動

プロテクションが動作することにより、故障箇所の診断に支障をきたすような場合は、次の方法によりプロテクションを解除した状態でダイアグモードに入ることができます。(過電流検出以外のプロテクション動作を解除する)

"TONE CONTROL" と "INFO" キーを押しながら "⏻" (電源) キーを押して電源を入れ、2つのキーと "⏻" (電源) キーを3秒以上押し続けます。

プロテクション解除モードでダイアグが起動します。

このモードではFLの"SLEEP"セグメントが点滅し、プロテクションを解除した状態でのダイアグモードであることを知らせます。

CAUTION!

Using this unit with the protection function disabled may cause further damage to this unit. Use special care for this point when using this mode.

注意！

プロテクションを解除した状態でのダイアグモードは、危険な状態でもプロテクションが作動しないため、動作させると、本機を破壊することがあります。このモードを使用する場合は十分注意してください。

● Canceling Self-Diagnostic Function

- Before canceling self-diagnostic function, execute setting for "S3. FACTORY PRESET" menu. (Memory initialization inhibited or Memory initialized).
 - * In order to keep the user memory preserved, be sure to select PRESET INHIBIT (Memory initialization inhibited).
- Press the "⏻" (Power) key to turn off the power.

● ダイアグの解除

- ダイアグを解除する前に、"S3. FACTORY PRESET" メニュー（メモリーの初期化禁止／またはメモリーの初期化）の設定をします。
 - ※ ユーザーメモリーを保持したい場合は、必ず PRESET INHIBIT（メモリー初期化禁止）を選択してください。
- "⏻"（電源）キーを押して電源を切ります。

● Display provided when Self-Diagnostic Function started

The display is as described below depending on the situation when the power to this unit is turned off.

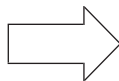
1. When the power is turned off by usual operation:

"NO PROTECT" is displayed. Then "A1-1. DSP MARGIN" is displayed in a few seconds.

Opening message / オープニング表示

NO PROTECT

After a few seconds / 数秒後



A1-1
DSP MARGIN

Main menu display / メインメニュー表示

● ダイアグ起動時の表示

本機の電源が切れたときの状況により、下記のように表示されます。

1. 通常の操作で電源を切った場合：

"NO PROTECT" が表示されます。数秒後、"A1-1. DSP MARGIN" が表示されます。

2. When the protection function worked to turn off the power:

The information of protection function which worked at that time is displayed. Then "A1-1. DSP MARGIN" is displayed in a few seconds.

Note: At that time if you restart the self-diagnostic function after turning off the power once, "NO PROTECT" will be displayed. That is because that situation is equal to "1. When the power is turned off by usual operation:".

However history of the protection function is stored in memory as backup data. For details, refer to "P2. PROTECTION HISTORY" menu.

2-1. When there is a history of protection function due to excess current.

I PROTECT

Cause: An excessive current flowed through the power amplifier.

Supplementary information: As current of the power amplifier is detected, the abnormal channel can be identified by checking the current detect transistor.

Turning on the power without correcting the abnormality will cause the protection function to work immediately and the power supply will instantly be shut off.

Notes:

- Applying the power to this unit without correcting the abnormality can be dangerous and cause additional circuit damage. To avoid this, if "I PROTECT" protection function works 1 time, the power will not turn on even when the "⏻" (Power) key is pressed. In order to turn on the power again, start up the self-diagnostic function.
- The output transistors in each amplifier channel should be checked for damage before applying power to this unit.
- Amplifier current should be monitored by measuring DC voltage across the emitter resistors for each channel.

2. プロテクションが働いて電源が切れた場合:

そのときに働いたプロテクションの情報が表示されます。数秒後、"A1-1. DSP MARGIN" が表示されます。

注) このとき、一旦電源を切った後にダイアグを再起動すると、"NO PROTECT" が表示されます。それは、その状況が「1. 通常の操作で電源を切った場合:」と同じだからです。

ただし、プロテクションの履歴はバックアップデータとしてメモリーに保存されます。詳細は、"P2. PROTECTION HISTORY" メニューを参照してください。

2-1. 過電流によるプロテクション履歴がある場合

原因: パワーアンプに過電流が流れた。

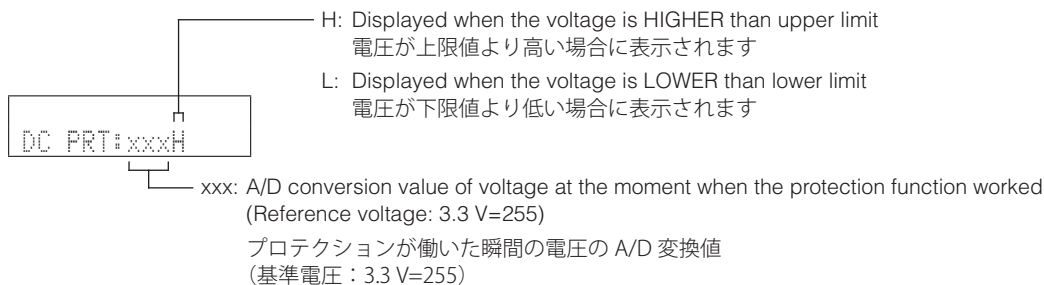
補足: パワーアンプの電流を検出していますので、電流検出トランジスタをチェックすれば異常チャンネルが特定できます。

異常状態のまま電源を入れると、瞬時にプロテクションが働き、すぐに電源が切れます。

注意:

- 異常状態のまま本機の電源を入れると、危険な状態になり、さらに回路が損傷を受ける原因になります。それを避けるために、「I PROTECT」が1回働いた場合、それ以降 "⏻" (電源) キーを押しても電源が入らなくなります。再度電源を入れる場合、ダイアグを起動してください。
- 本機の電源をいれる前に、各パワーアンプの出力トランジスタに損傷がないかチェックしてください。
- パワーアンプの電流は、各チャンネルのエミッターの抵抗器間 DC 電圧を測定することによりモニターしてください。

2-2. When the protection function worked due to abnormal DC output.



Cause: DC output of the power amplifier is abnormal.

Supplementary information: The protection function worked due to a DC voltage appearing at the speaker terminal. A cause could be a defect in the amplifier.

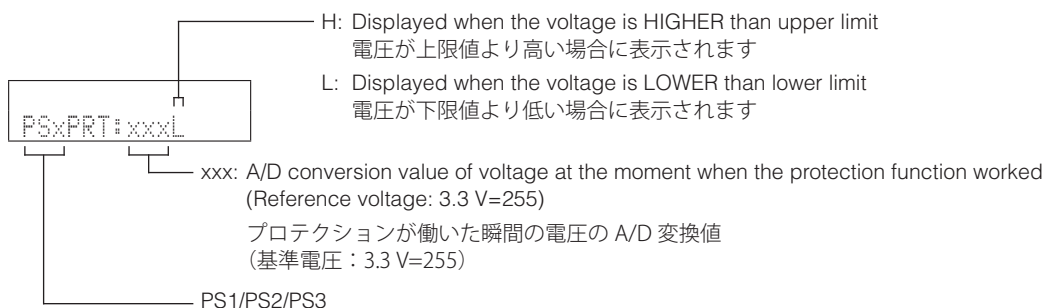
Turning on the power without correcting the abnormality will cause the protection function to work in 5 seconds and the power supply will be shut off.

原因: パワーアンプの DC 出力が異常。

補足: アンプの故障でスピーカー端子に直流電圧が掛かるなどが原因で、プロテクションが働いたことを示します。

異常状態のまま電源を入れると、5 秒後にプロテクションが働き、電源が切れます。

2-3. When the protection function worked due to abnormal voltage in the power supply section.



Cause: The voltage in the power supply section is abnormal.

Supplementary information: The protection function worked due to a defect or overload in the power supply.

Turning on the power without correcting the abnormality will cause the protection function to work in 1 seconds and the power supply will be shut off.

2-3. 電源部の電圧異常によりプロテクションが働いた場合

原因: 電源部の電圧が異常。

補足: 電源電圧による原因で、プロテクションが働いたことを示します。

異常状態のまま電源を入れると、1 秒後にプロテクションが働き、電源が切れます。

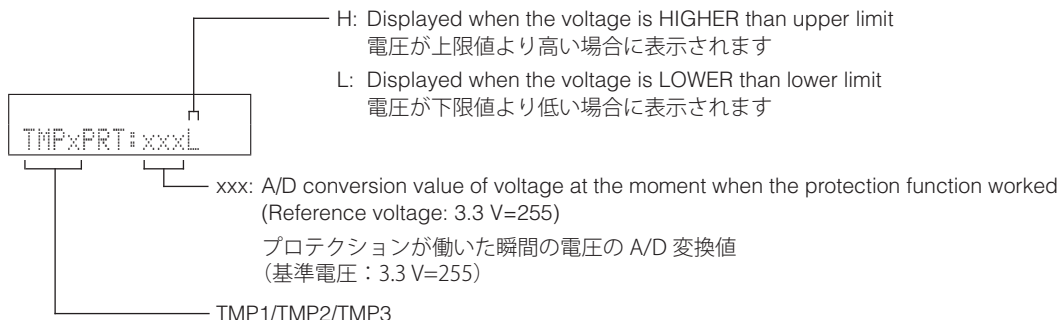
Notes:

- Applying the power to this unit without correcting the abnormality can be dangerous and cause additional circuit damage. To avoid this, if "PS" and "DC" protection function works 3 times consecutively, the power will not turn on even when the "⏻" (Power) key is pressed. In order to turn on the power again, start up the self-diagnostic function.
- The output transistors in each amplifier channel should be checked for damage before applying power to this unit.
- Amplifier current should be monitored by measuring DC voltage across the emitter resistors for each channel.

注意:

- 異常状態のまま本機の電源を入れると、危険な状態になり、さらに回路が損傷を受ける原因になります。それを避けるために、「DC」、「PS」プロテクションが連続して3回目働いた場合、それ以降「⏻」（電源）キーを押しても電源が入らなくなります。再度電源を入れる場合、ダイアグを起動してください。
- 本機の電源をいれる前に、各パワーアンプの出力トランジスタに損傷がないかチェックしてください。
- パワーアンプの電流は、各チャンネルのエミッターの抵抗器間 DC 電圧を測定することによりモニターしてください。

2-4. When the protection function worked due to excessive heatsink temperature.



Cause: The temperature of the heatsink is excessive.

Supplementary information: The protection function worked due to the temperature limit being exceeded. Causes could be poor ventilation or a defect related to the thermal sensor.

Turning on the power without correcting the abnormality will cause the protection function to work in 1 seconds and the power supply will be shut off.

2-4. ヒートシンクの異常温度によりプロテクションが働いた場合

原因: ヒートシンクの温度が異常。

補足: 温度制限を越えた原因で、プロテクションが働いたことを示します。

異常状態のまま電源を入れると、1 秒後にプロテクションが働き、電源が切れます。

● History of protection function

When the protection function has worked, its history is stored in memory as backup data.

Even if no abnormality is noted while servicing the unit, an abnormality which has occurred previously can be defined as long as the backup data has been stored.

For details, refer to "P2. PROTECTION HISTORY" menu.

● プロテクションの履歴

プロテクションが働いた場合、その履歴はバックアップデータとしてメモリーに保存されます。

修理のときに異常が認められなくても、バックアップデータが残っていれば、お客様のところで起きた異常を区別できます。

詳細は、"P2. PROTECTION HISTORY" メニューを参照してください。

● Operation procedure of Main menu and Sub-menu

There are 27 main menu items, each of which has sub-menu items.

Main menu selection

Select the main menu using "SCENE TV" (forward) and "SCENE BD/DVD" (reverse) keys.

Sub-menu selection

Select the sub-menu using "SCENE RADIO" (forward) and "SCENE NET" (reverse) keys.

● メインメニューとサブメニューの操作

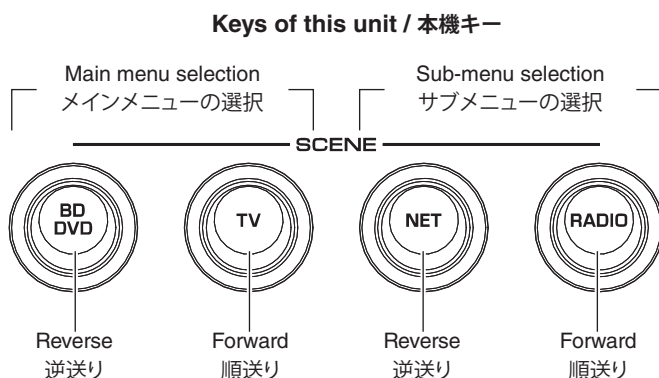
ダイアグには 27 個のメインメニューがあり、そのそれぞれにサブメニューがあります。

メインメニューの選択

"SCENE TV" (順送り)、"SCENE BD/DVD" (逆送り) キーで選択します。

サブメニューの選択

"SCENE RADIO" (順送り)、"SCENE NET" (逆送り) キーで選択します。



● Functions in Self-Diagnostic Function mode

In addition to the self-diagnostic function menu items, functions listed below are available.

- Power ON/OFF
- Master volume
- Muting
- Input selection

* Functions related to the tuner and the set menu are not available.

● ダイアグ中の機能

ダイアグメニューの他に、以下の機能が動作します。

- 電源 オン/オフ
- マスターボリューム
- ミュート
- インプットセレクト

※ チューナー関連、セットメニュー関連は機能しません。

● Initial settings when Self-Diagnostic Function started

The following initial settings are used when self-diagnostic function is started.

When self-diagnostic function is canceled, these settings are restored to those before starting self-diagnostic function.

- Master volume: -20 dB
- Input: AV1
- Speaker setting: LARGE, Bass out to SWFR (All channels)
- HDMI Control: Off

● ダイアグ開始時の初期設定

ダイアグ開始時に以下のような設定になります。

ダイアグ解除時にはダイアグ開始前の状態に戻ります。

- マスターボリューム: -20 dB
- インプット: AV1
- スピーカー設定: LARGE、Bass out to SWFR (すべてのチャンネル)
- HDMI コントロール: OFF

● Details of Self-Diagnostic Function menu

A1. DSP AUDIO

This menu is used to check audio signal route via DSP.

A1-1. DSP MARGIN

The audio signal is output including the head margin via DSP.

* When input source is stereo, signal is assigned as below.

Front L: Front L, Center, Surround L

Front R: Front R, Surround R

Front L +10 dB: Subwoofer

```
A1-1
DSP MARGIN
```

A1-2. DSP NON MARGIN

The SUBWOOFER signal is output including the head margin via DSP.

The audio signal other than SUBWOOFER is output without including the head margin via DSP.

```
A1-2
DSP NON MARGIN
```

A1-3. DSP FULL CENTER

The audio signal is output to only CENTER channel in digital full bit without including the head margin.

```
A1-3
DSP FULL C
```

A1-4. DSP FULL SURROUND

The audio signal is output to only SURROUND L/R channels in digital full bit without including the head margin.

```
A1-4
DSP FULL SUR
```

● ダイアグメニュー詳細

A1. DSP AUDIO

DSP を経由する音声信号の経路をチェックします。

A1-1. DSP MARGIN

音声信号が DSP を経由してヘッドマージンを含んで出力されます。

※ 2ch 信号入力時、以下のように信号が振り分けられて出力されます。

Front L : Front L、Center、Surround L

Front R : Front R、Surround R

Front L +10 dB : Subwoofer

A1-2. DSP NON MARGIN

サブウーファースの音声信号が DSP を経由してヘッドマージンを含んで出力されます。

サブウーファー以外の音声信号は DSP を経由してヘッドマージンを含まず出力されます。

A1-3. DSP FULL CENTER

音声信号がヘッドマージンを含まず、デジタルフルビットで CENTER チャンネルのみへ出力されます。

A1-4. DSP FULL SURROUND

音声信号がヘッドマージンを含まず、デジタルフルビットで SURROUND L/R チャンネルのみへ出力されます。

A1-5. DSP FULL SURROUND BACK

Not for service.

A1-5. DSP FULL SURROUND BACK

サービスでは使用しません。

```
A1-5
DSP FULL SB
```

A1-6. DSP FULL SUBWOOFER

The audio signal is output to only SUBWOOFER channel in digital full bit without including the head margin.

A1-6. DSP FULL SUBWOOFER

音声信号がヘッドマージンを含まず、デジタルフルビットで SUBWOOFER チャンネルのみへ出力されます。

```
A1-6
DSP FULL SW
```

A2. DIRECT AUDIO

This menu is used to check audio signal route of DIRECT mode.

A2. DIRECT AUDIO

DIRECT モードの音声信号の経路をチェックします。

A2-1. ANALOG DIRECT

The analog input audio signal is output to FRONT L and FRONT R channels in DIRECT mode.

A2-1. ANALOG DIRECT

アナログ入力の音声信号が DIRECT モードで FRONT L、FRONT R チャンネルへ出力されます。

```
A2-1
ANALOG DIRECT
```

A2-2. NET DIRECT

Not for service.

A2-2. NET DIRECT

サービスでは使用しません。

```
A2-2
NET DIRECT
```

A3. HDMI AUDIO

This menu is used to check the route of audio signal input to HDMI IN/OUT jack.

- * Before check using "A3-2. ARC" menu, be sure to connect a TV monitor equipped with Audio Return Channel function to this unit in advance.

A3-1
HDMI AUTO



A3-2
ARC

A3-1. HDMI AUTO

The audio signal input to selected HDMI IN jack is output.

選択された HDMI IN 端子へ入力された音声信号が出力されます。

A3-2. ARC (Audio Return Channel function)

The audio signal input to HDMI OUT jack is output.

HDMI OUT 端子へ入力された音声信号が出力されます。

A3. HDMI AUDIO

HDMI IN/OUT 端子へ入力された音声信号の経路をチェックします。

- ※ "A3-2. ARC" メニューでのチェックの前に、あらかじめ必ず Audio Return Channel 機能に対応しているテレビを接続してください。

A4. SPEAKERS SET

This menu is used to check the speaker output.

A4-1
FULL MUTE



A4-2
BI-AMP



A4-3
AC_B:Hi



A4-4
AC_B:Lo

A4-1. FULL MUTE

The audio signals are muted at all channels.

音声信号がすべてのチャンネルでミュートされます。

A4-2. BI-AMP

Not for service.

サービスでは使用しません。

A4-3. AC B HIGH

Not for service.

サービスでは使用しません。

A4-4. AC B LOW

Not for service.

サービスでは使用しません。

A4. SPEAKERS SET

スピーカー出力をチェックします。

A5. MIC CHECK

A5-1. MIC ROUTE CHECK

The audio signal input to the YPAO MIC jack is output to FRONT L channels via A/D-D/A.

A5-1
MIC ROUTE ON

ON: Connected / 接続されている
OFF: Unconnected / 接続されていない

A6. INVALID ITEM

Not for service.

A6-1
Invalidity

.....

A6-3
Invalidity

A5. MIC CHECK

A5-1. MIC ROUTE CHECK

YPAO マイク端子へ入力された音声信号が A/DーD/A 経由で FRONT L チャンネルへ出力されます。

A6. INVALID ITEM

サービスでは使用しません。

A7. DIR PLL (Phase Lock Loop)

This menu is used to check the route of digital audio signal input to AV1/AV2/AV3/AV4 jack.

A7-1
DIR PLL: ---

Lock: Lock / 同期
Unlock: Unlock / 非同期
---: Unconnected / 接続されていない

A7. DIR PLL (Phase Lock Loop)

AV1/AV2/AV3/AV4 端子へ入力されたデジタル音声信号の経路をチェックします。

A8. MANUAL TEST

The test noise generated by built-in noise generator in DSP is output to the channels specified by the sub-menu.

	Test noise / テストノイズ
for SUBWOOFER / SUBWOOFER 用	30 Hz to 80 Hz pink noise / ピンクノイズ
for other than SUBWOOFER / SUBWOOFER 以外	500 Hz to 2 kHz pink noise / ピンクノイズ

A8-1. TEST ALL

The test noise is output to all channels.

A8-1
TEST ALL

A8. MANUAL TEST

DSP に内蔵されたノイズジェネレータによって生成されたテストノイズが、サブメニューで指定したチャンネルへ出力されます。

A8-1. TEST ALL

テストノイズが全てのチャンネルへ出力されます。

H1. INVALID ITEM

Not for service.

H1-1
Invalidity

.....

H1-2
Invalidity

H1. INVALID ITEM

サービスでは使用しません。

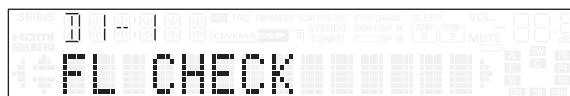
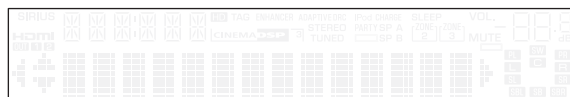
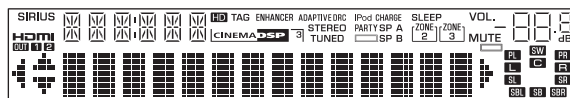
RX-V475/HTR-4066/
RX-V500D

D1. FL CHECK

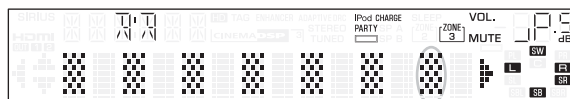
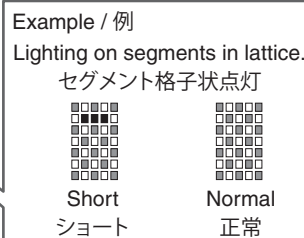
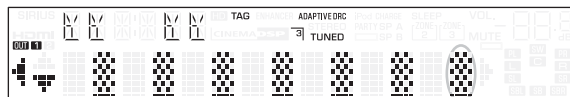
This menu is used to check operation of the FL display.

D1. FL CHECK

FL 表示の動作をチェックします。

FL display / FL 表示**D1-1. INITIAL DISPLAY / 初期表示****D1-2. ALL SEGMENT OFF / 全セグメント消灯****D1-3. ALL SEGMENT ON / 全セグメント点灯**

* After check, change to next menu at once.
確認後、すみやかに次のサブメニューを選択してください。

D1-4. CHECK PATTERN 1 / チェックパターン 1**D1-5. CHECK PATTERN 2 / チェックパターン 2**

Segment conditions of the FL tube is checked by turning ON and OFF all segments.

Next, a short between segments next to each other is checked by turning ON and OFF all segments alternately (in lattice).

(In the above example, the segments in the second row from the top are shorted.)

全セグメント消灯・全セグメント点灯により FL 管のセグメントの不良を確認します。

次に、全セグメントを交互（格子状）に点灯／消灯することで、隣り合うセグメントのショートをチェックします。

（上記の例は、上から 2 列目のセグメントがショートしています。）

U1. USB

This menu is used to check the audio signal route from USB storage device.

U1-1. USB FRONT 1 TRACK

The 1st music file stored in the USB storage device connected to the USB jack is reproduced.

- * Copy 2 or more music files from PC to the root folder of the USB storage device in advance.

```
U1-1
USB_F 1 TRACK
```

U1-2. USB BOOT

Not for service.

```
U1-2
USB BOOT:---
```

U1-3. USB_VBUS HIGH POWER

Not for service.

```
U1-3
USB_VBUS_HPWR
```

U1-4. INVALID ITEM

Not for service.

```
U1-4
Invalidity
```

U1. USB

USB フラッシュメモリーからの音声信号の経路をチェックします。

U1-1. USB FRONT 1 TRACK

USB 端子に接続された USB フラッシュメモリーに保存された音楽ファイルの 1 曲目が再生されます。

- ※ あらかじめ PC から USB フラッシュメモリーのルートフォルダに音楽ファイルを 2 曲以上コピーしてください。

U1-2. USB BOOT

サービスでは使用しません。

U1-3. USB_VBUS HIGH POWER

サービスでは使用しません。

U1-4. INVALID ITEM

サービスでは使用しません。

N1. NETWORK

This menu is used to check functions related to NETWORK.

Connect between LAN port of broadband router and NETWORK jack of this unit with a network cable.

- * When the network condition varies while sub-menu is displayed (e.g., the network is deactivated once), the correct result will not be displayed. In that case, once turn off the power to this unit, then start up the self-diagnostic function again and select this menu.

N1-1. IP ADDRESS CHECK

This menu is used to check that IP address can be obtained.

```
N1-1
IP AD CHK:OK
```

OK: Connected (IP address obtained)
接続 (IP アドレス取得完了)

NG: No traffic / Disconnected
通信不能 / 接続が切れている

N1-2. MAC ADDRESS CHECK

This menu is used to check that MAC address is written.

```
N1-2
MAC AD CHK:OK
```

OK: Normal / 正常

NG: Unwritten / 書き込まれていない

N1-3. LINE NOISE 100 MDI

Not for service.

N1-3. LINE NOISE 100 MDI

サービスでは使用しません。

```
N1-3
LN MDI 100
```

N1-4. LINE NOISE 100 MDIX

Not for service.

N1-4. LINE NOISE 100 MDIX

サービスでは使用しません。

```
N1-4
LN MDIX 100
```

N1.NETWORK

ネットワークに関連する機能をチェックします。

ブロードバンドルーターの LAN ポートと本機の NETWORK 端子をネットワークケーブルで接続します。

- ※ サブメニュー表示中にネットワークの状態が変わると (たとえばネットワークが一時切れるなど) 正しい結果が表示されません。その場合、一度本機の電源を切り、ダイアグを再起動して本メニューを選択します。

N1-1. IP ADDRESS CHECK

IP アドレスが取得されていることをチェックします。

N1-2. MAC ADDRESS CHECK

MAC アドレスが書き込まれていることをチェックします。

N1-5. LINE NOISE 10 MDI

Not for service.

```
N1-5
LN MDI 10
```

N1-5. LINE NOISE 10 MDI

サービスでは使用しません。

N1-6. LINE NOISE 10 MDIX

Not for service.

```
N1-6
LN MDIX 10
```

N1-6. LINE NOISE 10 MDIX

サービスでは使用しません。

N1-7. LINK CHECK

This menu is used to check that the broadband router is connected correctly.

```
N1-7
LINK CHK:OK
```

N1-7. LINK CHECK

ブロードバンドルーターが正しく接続されていることをチェックします。

OK: Connected / 接続

NG: No traffic / Disconnected

通信不能 / 接続が切れている

N1-8. EXT TEST

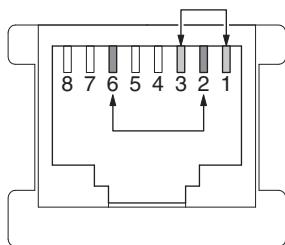
Transmission/reception of the NETWORK port is checked.

With the power turned off, short the pins of the NETWORK jack as shown in the figure below.

Start up the self-diagnostic function and select this menu.

Transmission/reception test is executed and its result is displayed.

Note) Be sure to return the shorted pins to their original condition after executing this test.



NETWORK jack

N1-8. EXT TEST

NETWORK ポートの送受信テストを行います。

電源を切った状態で、下図のように NETWORK 端子のピンをショートさせます。

ダイヤグを起動して本メニューを選択します。

送受信テストを行い、その結果が表示されます。

注意) 検査後、ショートしたピンを必ず元の状態に戻してください。

```
N1-8
EXT TEST:OK
```

OK: Normal / 正常

NG: Abnormal / 異常

--: Checking / チェック中

C1. DIGITAL P.C.B. CHECK

This menu is used to check the communication and bus line connection between devices on DIGITAL P.C.B.

C1-1. ALL

The total detection result of sub-menus from C1-2 to C1-8 is displayed.



```

C1-1
ALL:OK
  
```

OK: No error detected / 不良検出なし
 NG: An error is detected / 不良検出あり
 --: Checking / チェック中

C1. DIGITAL P.C.B. CHECK

DIGITAL P.C.B. 上の各デバイス間の通信とバスライン接続をチェックします。

C1-1. ALL

サブメニュー C1-2 ～ C1-8 の総合判定結果が表示されます。

C1-2. MCPU OSD

Microprocessor (IC21) and OSD FLASH ROM (IC2)'s reading/writing are checked.



```

C1-2
MCPU OSD:OK
  
```

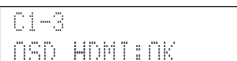
OK: No error detected / 不良検出なし
 NG: An error is detected / 不良検出あり

C1-2. MCPU OSD

マイコン (IC21) と OSD FLASH ROM (IC2) の読み出し／書き込みをチェックします。

C1-3. OSD HDMI

OSD FLASH ROM (IC2) and HDMI IC (IC1)'s reading/writing are checked.



```

C1-3
OSD HDMI:OK
  
```

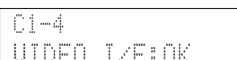
OK: No error detected / 不良検出なし
 NG: An error is detected / 不良検出あり

C1-3. OSD HDMI

OSD FLASH ROM (IC2) と HDMI IC (IC1) の読み出し／書き込みをチェックします。

C1-4. VIDEO I/F

Communication and bus line connection between microprocessor (IC21) and Video Selector (IC502) are checked.



```

C1-4
VIDEO I/F:OK
  
```

OK: No error detected / 不良検出なし
 NG: An error is detected / 不良検出あり
 --: Checking / チェック中

C1-4. VIDEO I/F

マイコン (IC21) と Video Selector (IC502) 間の通信とバスライン接続をチェックします。

C1-5. BUS DIR

Communication and bus line connection between microprocessor (IC21) and DIR (IC61) are checked.

C1-5. BUS DIR

マイコン (IC21) と DIR (IC61) 間の通信とバスライン接続をチェックします。

```
C1-5
DIR BUS:OK
```

OK: No error detected / 不良検出なし

NG: An error is detected / 不良検出あり

--: Checking / チェック中

C1-6. BUS DSP

Communication and bus line connection between microprocessor (IC21) and DSP (IC41) are checked.

C1-6. BUS DSP

マイコン (IC21) と DSP (IC41) 間の通信とバスライン接続をチェックします。

```
C1-6
DSP BUS:OK
```

OK: No error detected / 不良検出なし

NG: An error is detected / 不良検出あり

--: Checking / チェック中

C1-7. EEPROM

EEPROM (IC22)'s reading/writing is checked.

C1-7. EEPROM

EEPROM (IC22) の読み出し／書き込みをチェックします。

```
C1-7
EEPROM:OK
```

OK: No error detected / 不良検出なし

NG: An error is detected / 不良検出あり

--: Checking / チェック中

C1-8. TUNER

The AM/FM (RX-V475/HTR-4066) / DAB (RX-V500D) TUNER I2C (Inter integrated circuit) bus line connection is checked.

C1-8. TUNER

AM/FM TUNER の I2C (Inter integrated circuit) バスライン接続をチェックします。

```
C1-8
TUNER:OK
```

OK: No error detected / 不良検出なし

NG: An error is detected / 不良検出あり

--: Checking / チェック中

C2. HDMI INFORMATION

This menu is used to display information about HDMI.

C2-1. HDMI MODEL NAME

The model name written to HDMI IC is displayed.



RX-V475
HTR-4066
RX-V500D

C2. HDMI INFORMATION

HDMI に関する情報が表示されます。

C2-1. HDMI MODEL NAME

HDMI IC に書き込まれているモデル名が表示されます。

C2-2. HDMI PRODUCT ID

Not for service.



C2-2. HDMI PRODUCT ID

サービスでは使用しません。

C3. NETWORK IC CHECK

This menu is used to check the communication and bus line connection between devices related to network.

C3-1. ALL

The total detection result of sub-menus from C3-2 to C3-4 is displayed.

```
C3-1
ALL:OK
```

OK: No error detected / 不良検出なし
 NG: An error is detected / 不良検出あり
 --: Checking / チェック中

C3-2. NET RAM

Communication and bus line connection between network microprocessor (IC951) and SDRAM (IC952) are checked.

```
C3-2
NET RAM:OK
```

OK: No error detected / 不良検出なし
 NG: An error is detected / 不良検出あり
 --: Checking / チェック中

C3-3. PHY (Ethernet PHYceiver) TEST

The perform a loopback test in PHY (IC955).

```
C3-3
PHY TEST:OK
```

OK: No error detected / 不良検出なし
 NG: An error is detected / 不良検出あり
 --: Checking / チェック中

C3-4. APL (Apple) ID CHECK

Apple authentication IC (IC956) device ID is checked.

```
C3-4
APL ID:OK
```

OK: No error detected / 不良検出なし
 NG: An error is detected / 不良検出あり
 --: Checking / チェック中

C3. NETWORK IC CHECK

ネットワークに関連する各デバイス間の通信とバスラインの接続をチェックします。

C3-1. ALL

サブメニュー C3-2 ～ C3-4 の総合判定結果が表示されます。

C3-2. NET RAM

ネットワークマイコン (IC951) と SDRAM (IC952) の通信とバスラインの接続チェックします。

C3-3. PHY (Ethernet PHYceiver) TEST

PHY (IC955) 内でループバックテストを行います。

C3-4. APL (Apple) ID CHECK

Apple 認証 IC (IC956) のデバイス ID をチェックします。

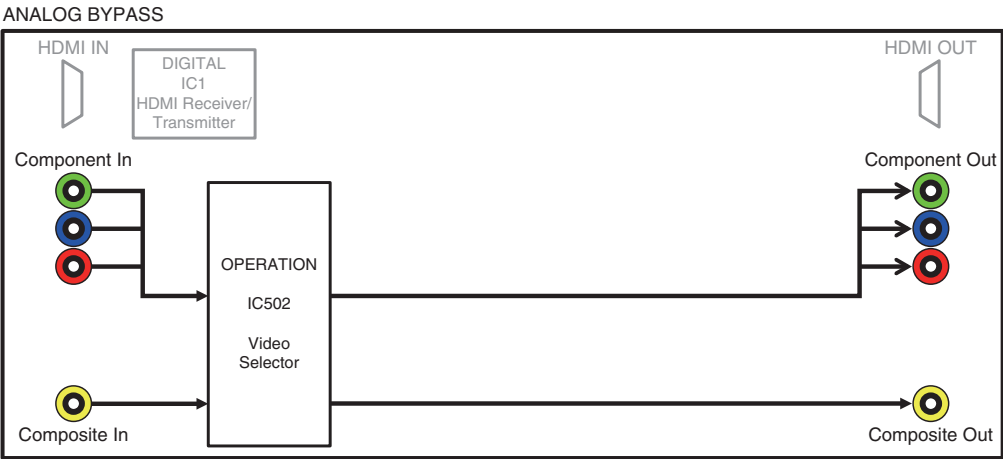
V1. ANALOG VIDEO CHECK

This menu is used to check the analog video signal route.

V1-1. ANALOG BYPASS

The video signal is output as shown below.

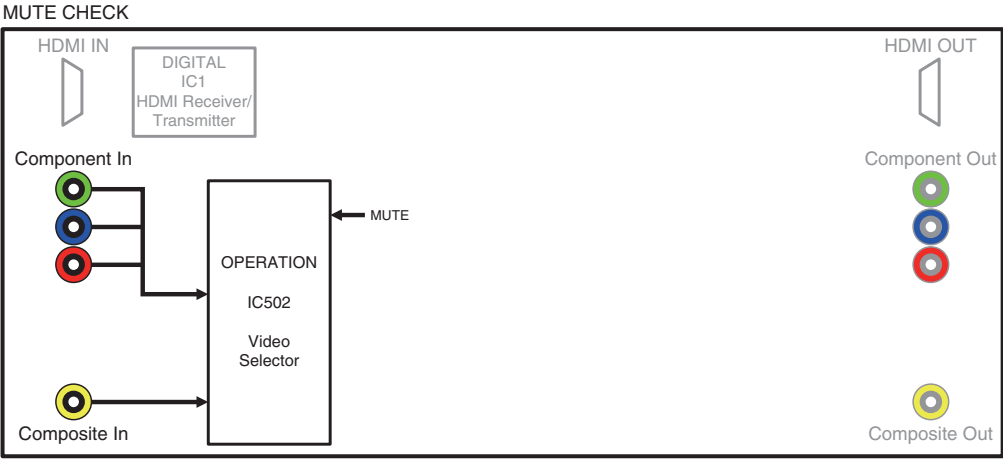
V1-1
ANALOG BYPASS



V1-2. MUTE CHECK

The video signal is muted.

V1-2
MUTE CHECK



V2. DIGITAL VIDEO CHECK

This menu is used to check the digital video signal route.

V2-1. HDMI REPEAT

The video/audio signals input to HDMI IN jack are output to HDMI OUT jack.

V2. DIGITAL VIDEO CHECK

デジタル映像信号の経路をチェックします。

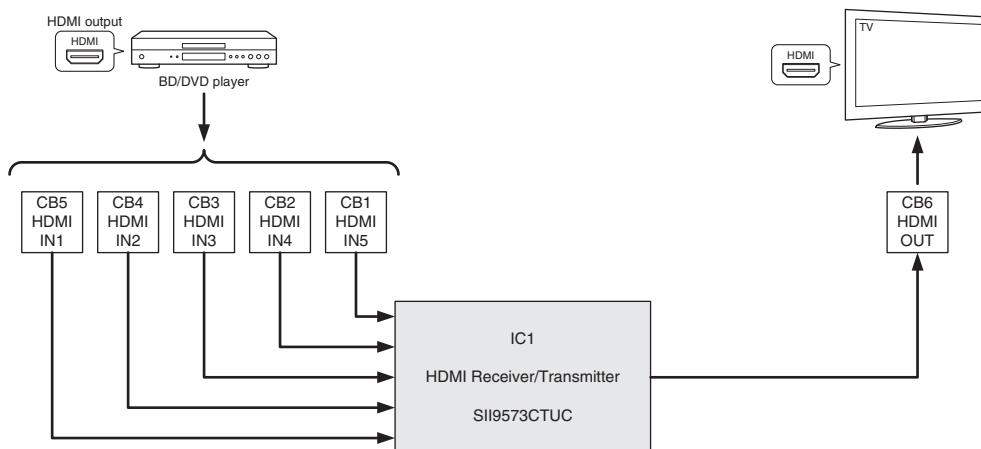
V2-1. HDMI REPEAT

HDMI IN 端子へ入力された映像信号と音声信号が HDMI OUT 端子へ出力されます。

V2-1
HDMI REPEAT **

The Deep Color video signals is input, "30" bit or "36" bit is displayed.

Deep Color 映像信号を入力すると、“30” bit または “36” bit が表示されます。



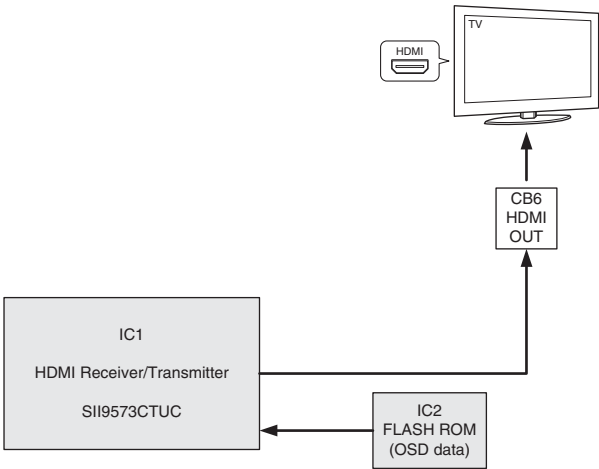
V2-2. OSD (On-Screen Display) VIDEO OUT

The “OSD CHECK” screen is output to HDMI OUT jack.

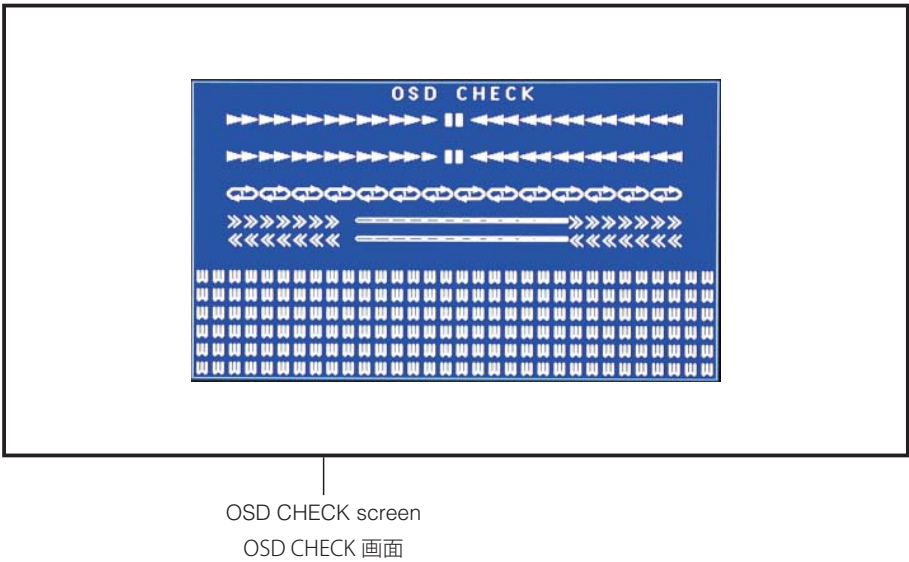
V2-2. OSD (On-Screen Display) VIDEO OUT

“OSD CHECK” 画面が HDMI OUT 端子へ出力されます。

V2-2
OSD-VIDEO OUT



TV screen display / TV 画面表示



R1. DAB (RX-V500D model)

This menu is used to display the DAB module information.

R1-1. SIGNAL QUALITY

Not for service.

```
R1-1
0
```

R1-2. DAB MODULE VERSION

The firmware version of DAB module is displayed.

```
R1-2
DAB: 21982.02
```

R1. DAB (RX-V500D model)

サービスでは使用しません。

```
R1-1
Invalidity
```

.....

```
R1-2
Invalidity
```

P1. SYSTEM MONITOR

This menu is used to display the A/D conversion value of the microprocessor which detects panel keys and protection functions by using the sub-menu.

When "P1-7. KEY1/KEY2" sub-menu is selected, keys become inoperable due to detection of the values of all keys. However, it is possible to advance to the next menu by turning the VOLUME knob.

- * Numeric values in the figure are given as reference only.

P1-1. DC

Power amplifier DC (DC voltage) output is detected.

The voltage at 120 pin (DC_PRT) of IC21 is displayed.

Normal value: 27 to 89

(Reference voltage: 3.3 V=255)

- * If DC becomes out of the normal value range, the protection function works to turn off the power.

```
P1-1
DC: 059
```

P1. SYSTEM MONITOR

パネルキー、プロテクションなどを検出しているマイコンの A/D 変換値を、サブメニューで表示します。サブメニュー "P1-7. KEY1/KEY2" にすると、全キーの値を検出するためキー操作はできなくなりますが、VOLUME ツマミを回すことにより、次のメニューに進めることができます。

※ 図中の数値は参考例です。

P1-1. DC

パワーアンプ DC (直流電圧) 出力の検出

IC21 の 120 ピン (DC_PRT) の電圧が表示されます。

正常値: 27 ~ 89

(基準電圧: 3.3 V=255)

※ DC が正常値を外れるとプロテクションが働き、電源が切れます。

P1-2. PS

Power supply voltage (PS) protection detection.

The voltage at 126 pin (PS1_PRT)/107 pin (PS2_PRT)/106 pin (PS3_PRT) of IC21 are displayed.

Voltage detects

PS1: AC_BL, AC_V, AC_12, $\pm 7A$, +3.3S

PS2: $\pm 12A$, +5A, $\pm 3.3V$, -VP

PS3: +5.5V

Normal value

PS1: 12 to 100

PS2: 34 to 106

PS3: 132 to 168

(Reference voltage: 3.3 V=255)

- * If PS1, PS2 or PS3 becomes out of the normal value range, the protection function works to turn off the power.

P1-2. PS

電源電圧 (PS) プロテクションの検出

IC21 の 126 ピン (PS1_PRT) / 107 ピン (PS2_PRT) / 106 ピン (PS3_PRT) の電圧が表示されます。

検出電圧

PS1 : AC_BL、AC_V、AC_12、 $\pm 7A$ 、+3.3S

PS2 : $\pm 12A$ 、+5A、 $\pm 3.3V$ 、-VP

PS3 : +5.5V

正常値

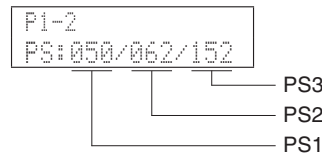
PS1 : 12 ~ 100

PS2 : 34 ~ 106

PS3 : 132 ~ 168

(基準電圧 : 3.3 V=255)

- ※ PS1、PS2 または PS3 が正常値を外れるとプロテクションが働き、電源が切れます。

**P1-3. TMP**

Temperature of the heatsink (THM) is detected.

The voltage at 122 pin (THM1_PRT)/123 pin (THM2_PRT) /110 pin (THM3_PRT) of IC21 is displayed.

Normal value

THM1: 42 to 255

THM2: 42 to 255 (U, C models)

THM3: 115 to 255

(Reference voltage: 3.3 V=255)

- * If THM1, THM2 or THM3 becomes out of the normal value range, the protection function works to turn off the power.

P1-3. TMP

ヒートシンク温度 (THM) の検出

IC21 の 122 ピン (THM1_PRT) / 123 ピン (THM2_PRT) / 110 ピン (THM3_PRT) の電圧が表示されます。

正常値

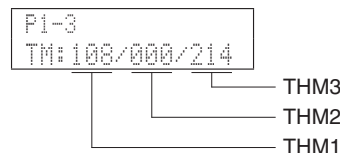
THM1 : 42 ~ 255

THM2 : (サービスでは使用しません。)

THM3 : 115 ~ 255

(基準電圧 : 3.3 V=255)

- ※ THM1、THM2 または THM3 が正常値を外れるとプロテクションが働き、電源が切れます。



P1-4. OUTPUT LEVEL

Output level of speaker output is detected.
The voltage at 121 pin (LMT_OLV) of IC21 is displayed.

(Reference voltage: 3.3 V=255)

```
P1-4
OUTLVL: 255
```

P1-4. OUTPUT LEVEL

スピーカー出力の出力レベルの検出
IC21 の 121 ピン (AMP_OLV) の電圧が表示されます。

(基準電圧：3.3 V=255)

P1-5. LIMITER CONTROL

Power limiter control is detected.
The voltage at 7 pin (AMP_LMT) of IC21 is displayed.

(Reference voltage: 3.3 V=255)

```
P1-5
LMTCNT: 255
```

P1-5. LIMITER CONTROL

電源リミッター制御の検出
IC21 の 7 ピン (AMP_LMT) の電圧が表示されます。

(基準電圧：3.3 V=255)

P1-6. USB-VBUS

Power supply voltage of USB jack is detected.
The voltage at 109 pin (USB_VBUS_PRT) of IC21 is detected.

(Reference voltage: 3.3 V=255)

```
P1-6
USB-VBUS:011
```

P1-6. USB-VBUS

USB 端子の電源電圧の検出
IC21 の 109 ピン (USB_VBUS_PRT) の電圧が表示されます。

(基準電圧：3.3 V=255)

P1-7. KEY

Panel key is detected.

When the A/D conversion value of the panel key becomes out of the specified range, normal operation will not be available.

In that case, check the constant of voltage dividing resistor, solder condition, etc. Refer to table.

* When “P1-7. KEY1/KEY2” menu is selected, keys become inoperable due to detection of the values of all keys. However, it is possible to advance to the next menu by turning the VOLUME knob.

(Reference voltage: 3.3 V=255)

P1-7. KEY

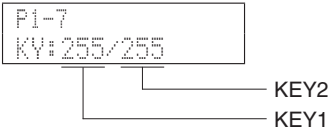
パネルキーの検出

パネルキーの A/D 値が規定範囲から外れると、正常な動きをしません。

下表をご覧になり、各キーの分圧抵抗の定数、ハンダ不良等の確認をしてください。

※ “P1-7. KEY1/KEY2” メニューにすると、全キーの値を検出するためキー操作はできなくなりますが、VOLUME ツマミを回すことにより、次のメニューに進めることができます。

(基準電圧：3.3 V=255)



Display / 表示	KEY1
0 – 11	RADIO (SCENE4)
12 – 32	NET (SCENE3)
33 – 54	TV (SCENE2)
55 – 75	BD/DVD (SCENE1)
76 – 96	–
97 – 119	–
120 – 142	INPUT >
143 – 163	INPUT <
182 – 197	⏻ (Power)
198 – 229	TONE CONTROL
255	Key off

Display / 表示	KEY2
0 – 11	DIRECT
12 – 32	TUNING >>
33 – 54	TUNING <<
55 – 77	AM (RX-V475/HTR-4066) DAB (RX-V500D)
78 – 99	FM
100 – 121	PRESET >
122 – 144	PRESET <
145 – 166	MEMORY
167 – 186	INFO
187 – 205	STRAIGHT
206 – 226	PROGRAM >
227 – 246	PROGRAM <
255	Key off

RX-V475/HTR-4066/
RX-V500D

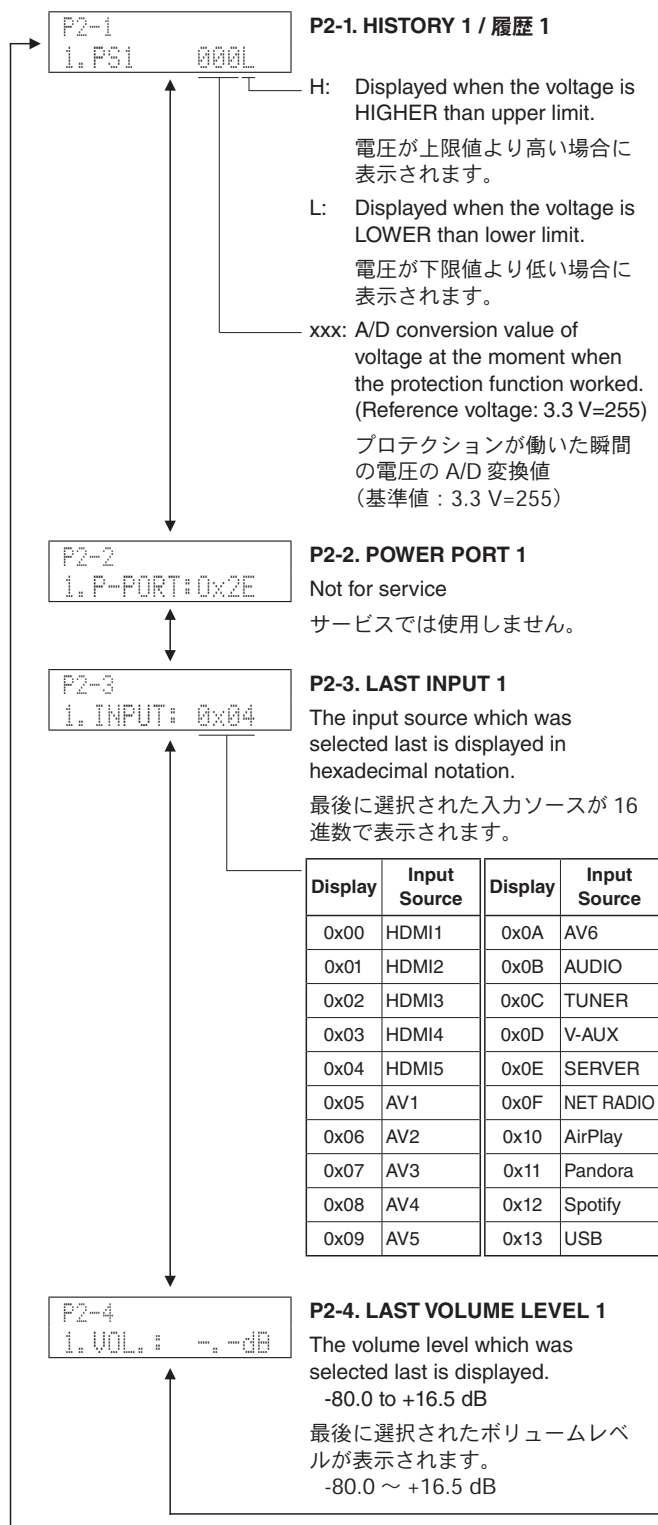
P2. PROTECTION HISTORY

This menu is used to display the history of protection function.

In the history 1 to 4, the setting information for operation of each protection function will be stored.

All history of protection function and setting information will be erased by pressing the "STRAIGHT" key.

* Numeric values in the figure are given as reference only.



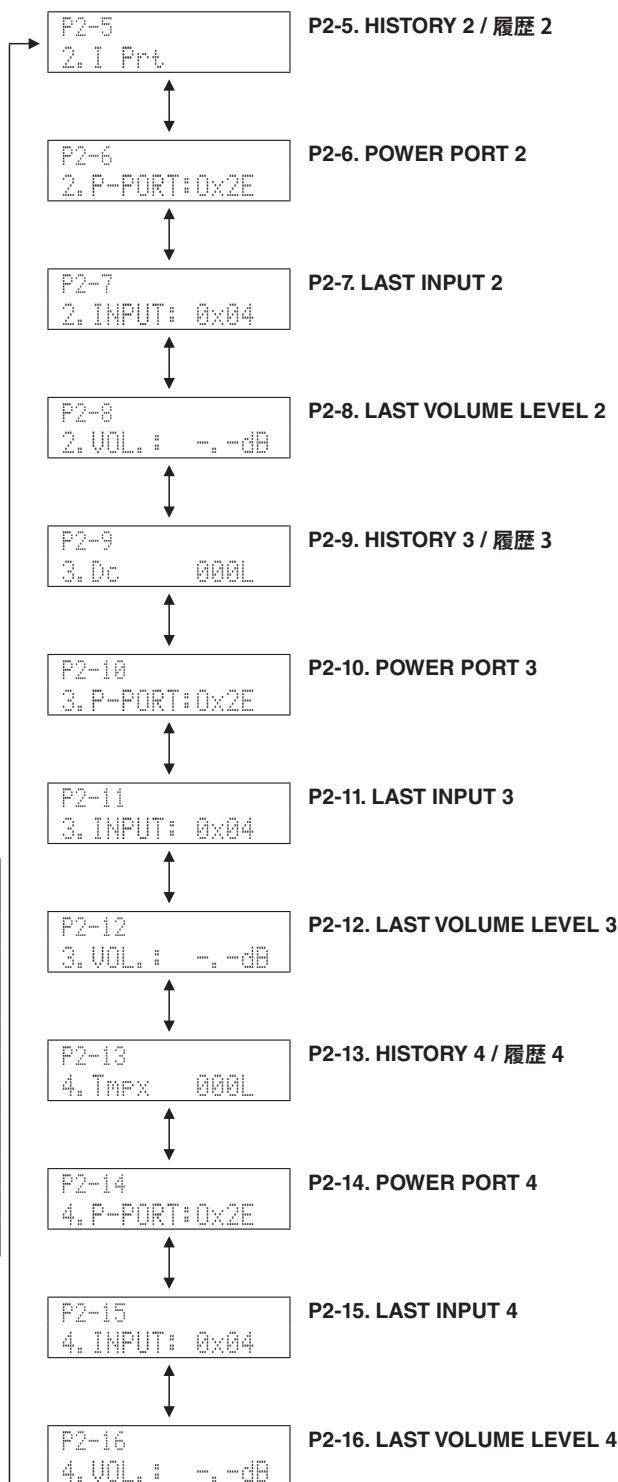
P2. PROTECTION HISTORY

プロテクション履歴が表示されます。

履歴 1 ~ 4 には、そのそれぞれにプロテクション動作時の設定情報が保存されます。

"STRAIGHT" キーを押すと、すべてのプロテクション履歴と、設定情報が消去されます。

※ 図中の数値は参考例です。



T1. TROUBLE SHOOTING INFORMATION

This menu is used to display the operating time and operation frequency of this unit.

* The operating time and operation frequency during the self-diagnostic function mode will not be stored.

T1-1. OPERATING TIME

The operating time of this unit is displayed.
The operating time will be erased by pressing the "STRAIGHT" key.



Minute (0M to 59M) / 分 (0M ~ 59M)
Hour (0H to 23H) / 時間 (0H ~ 23H)
Day (0D to 9999D) / 日数 (0D ~ 9999D)

T1-2. POWER-RELAY ON

The operation frequency of the power relay (RY541) is displayed in hexadecimal notation.
The operation frequency will be erased by pressing the "STRAIGHT" key.



Operation frequency / 0 to FFFF (up to 65,535 times)
動作回数 / 0 ~ FFFF (最大 65,535 回)

T1-3. POWER AMP B

The operation frequency of the POWER AMP B relay (RY206) is displayed in hexadecimal notation.
The operation frequency will be erased by pressing the "STRAIGHT" key.



Operation frequency / 0 to FF (up to 255 times)
動作回数 / 0 ~ FF (最大 255 回)

T1-4. OUTPUT LEVEL

The maximum value of the speaker output level is displayed in hexadecimal notation.
The maximum value will be erased by pressing the "STRAIGHT" key.



Maximum value / 0 to FF
最大値 / 0 ~ FF

T1-5. NRC (Net Restart Counter)

Not for service.



T1. TROUBLE SHOOTING INFORMATION

本機の動作時間、動作回数が表示されます。

※ ダイアグ中の動作時間、動作回数は保存されません。

T1-1. OPERATING TIME

本機の動作時間が表示されます。
"STRAIGHT" キーを押すと動作時間が消去されます。

T1-2. POWER-RELAY ON

電源リレー (RY541) の動作回数が 16 進数で表示されます。
"STRAIGHT" キーを押すと動作回数が消去されます。

T1-3. POWER AMP B

POWER AMP B リレー (RY206) の動作回数が 16 進数で表示されます。
"STRAIGHT" キーを押すと動作回数が消去されます。

T1-4. OUTPUT LEVEL

スピーカー出力レベルの最大値が 16 進数で表示されます。
"STRAIGHT" キーを押すと最大値が消去されます。

T1-5. NRC (Net Restart Counter)

サービスでは使用しません。

RX-V475/HTR-4066/
RX-V500D

S1. FIRMWARE UPDATE

Not for service.



S1. FIRMWARE UPDATE

サービスでは使用しません。

S2. SET INFORMATION

This menu is used to display the model name and destination.

S2-1. INITIAL DISPLAY



S2. SET INFORMATION

モデル名、仕向け先が表示されます。

S2-1. INITIAL DISPLAY

S2-2. MODEL/DESTINATION

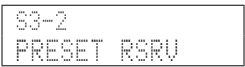
The model name and destination are displayed.



Not for service / サービスでは使用しません
Destination / 仕向け先
U / C / R (R, S) / T / K / A / G (B, G, F) / L (L, H) / J
Model name / モデル名
V475 : RX-V475
H4066 : HTR-4066
V500D : RX-V500D

S3. FACTORY PRESET

This menu is used to reserve/inhibit initialization of the back-up IC (EEPROM: IC22 on DIGITAL P.C.B.).



S3-1. PRESET INHIBIT (Initialization inhibited) / PRESET INHIBIT (初期化禁止)

Initialization of the back-up IC is not executed. Select this sub-menu to protect the values set by the user.
バックアップ用 IC の初期化は行われません。ユーザーの設定値を保護するときは、こちらを選択してください。

S3-2. PRESET RESERVED (Initialization reserved) / PRESET RESERVED (初期化予約)

Initialization of the back-up IC is reserved. (Actual initialization is executed when the power is turned on next.) To reset to the original factory settings or to reset the backup IC, select this sub-menu and press the "P" (Power) key to turn off the power.

ユーザーメモリーの初期化が予約されます。(実際に初期化されるのは、次の電源投入時です。)工場出荷時やユーザーメモリーをリセットしたいときは、こちらを選択してから "P" (電源) キーを押して電源を切ってください。

CAUTION: Before setting to the PRESET RESERVED, write down the existing preset memory content of the tuner. (This is because setting to the PRESET RESERVED will cause the user memory content to be erased.)

S3. FACTORY PRESET

バックアップ IC (EEPROM : DIGITAL P.C.B. の IC22) の初期化を予約／禁止します。

注意： PRESET RESERVED を選んで初期化をする前に、チューナーのユーザーメモリーの内容を書き写してください。(初期化をすると、チューナーのユーザーメモリーの内容は消えてしまいます。)

S4. ROM VERSION/CHECKSUM

The firmware version and checksum values are displayed.

The checksum is obtained by adding the data at every 8-bit and expressing the result as a hexadecimal notation.

* Numeric values in the figure are given as reference only.

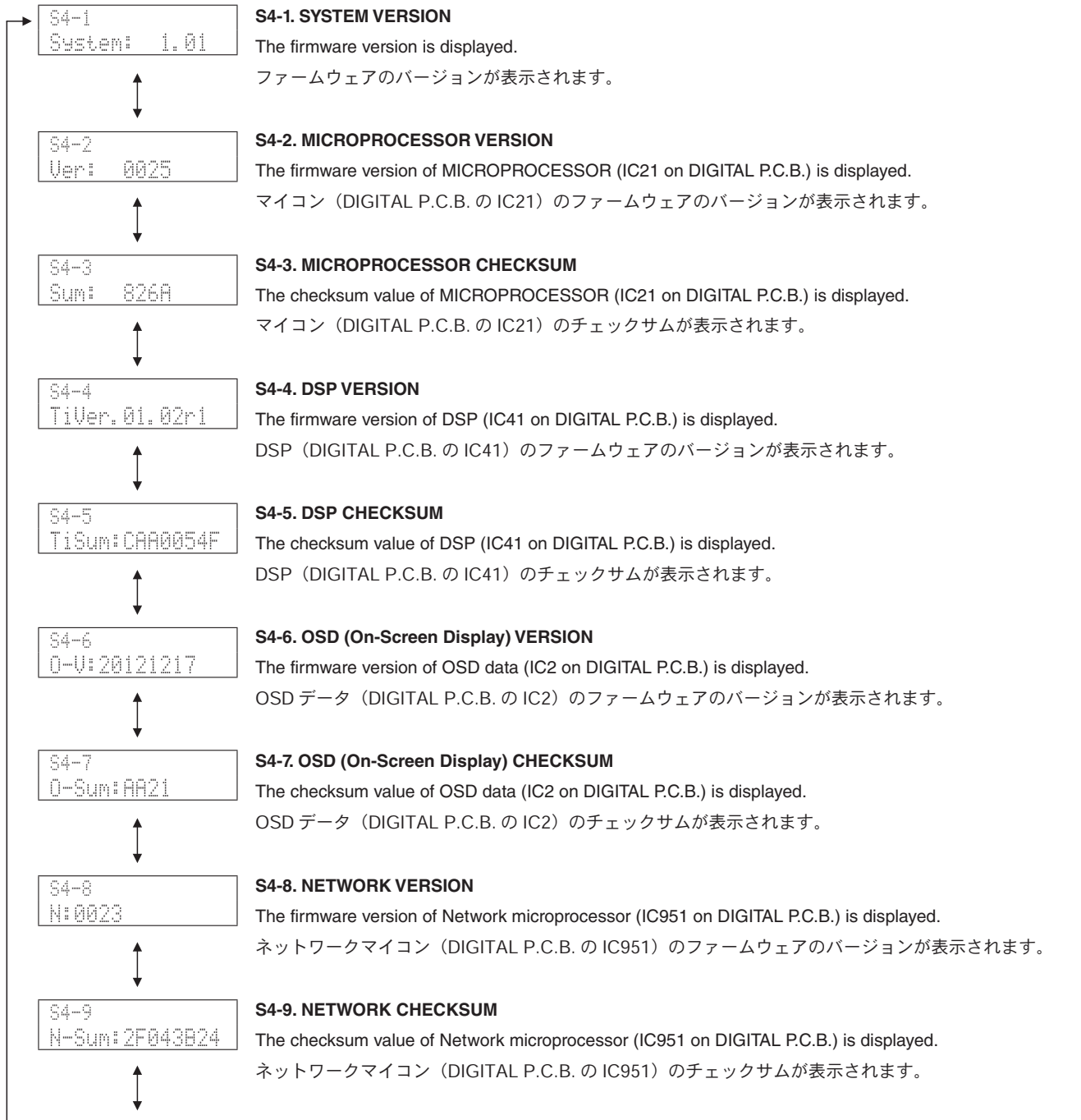
S4. ROM VERSION/CHECKSUM

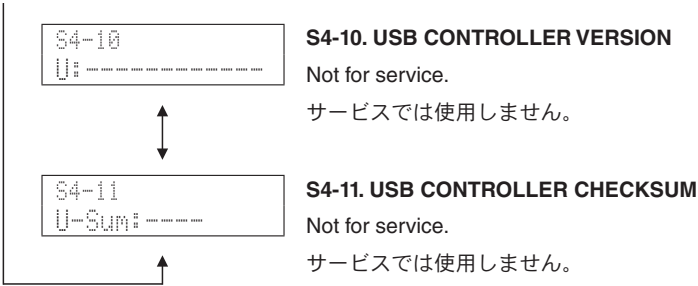
ファームウェアのバージョン、チェックサムが表示されます。

チェックサムは、データを8ビットごとに加算していき、16進数で表記したものです。

※ 図中の数値は参考例です。

RX-V475/HTR-4066/
RX-V500D





S5. SOFT SWITCH (RX-V475/HTR-4066 models)

This menu is used to write the model name to the back-up IC (EEPROM: IC22 on DIGITAL P.C.B.).

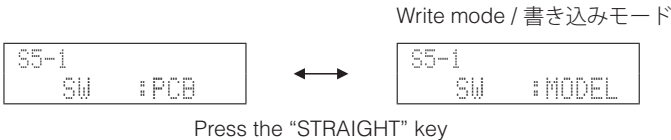
When the following parts are replaced, the model name MUST be written by using this menu to have proper operation.

DIGITAL P.C.B.
EEPROM: IC22 on DIGITAL P.C.B.

To write the model name, first switch to the write mode by using the “S5-1. SWITCH MODE” menu and then select the desired model name by using “S5-2. MODEL NAME” menu.

S5-1. SWITCH MODE

Pressing the “STRAIGHT” key will change the display alternately as shown below. When “S5-1. SW: MODEL” is displayed, this unit is in the write mode.



Note: After writing of the model name is completed, be sure to change to “S5-1. SW: PCB”.

S5. SOFT SWITCH

モデル名をバックアップIC (EEPROM: DIGITAL P.C.B.のIC22) に書き込みます。

下記の部品を交換した場合、正常動作のために本メニューでモデル名を書き込む必要があります。

DIGITAL P.C.B.
EEPROM : DIGITAL P.C.B. の IC22

モデル名を書き込むには、まず最初に “S5-1. SWITCH MODE” メニューで書き込みモードに切り替えて、それから “S5-2. MODEL NAME” メニューで目的のモデル名を選択します。

S5-1. SWITCH MODE

“STRAIGHT” キーを押すと表示が下記のように交互に切り替わります。“S5-1. SW: MODEL” が表示されているときに本機は書き込みモードになっています。

注意： モデル名の書き込みを完了した後、必ず “S5-1. SW: PCB” に切り替えてください。

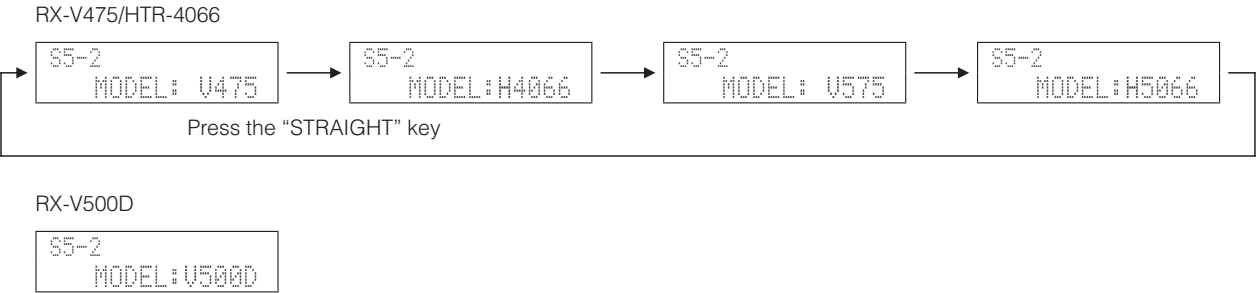
RX-V475/HTR-4066/
RX-V500D

S5-2. MODEL NAME

Select the desired model name by pressing the "STRAIGHT" key. Then the selected model name is written automatically.

S5-2. MODEL NAME

"STRAIGHT" キーを押して目的のモデル名を選択します。選択されたモデル名が自動的に書き込まれます。



S6. SYSTEM INFORMATION

This menu is used to display the model name and destination.

S6. SYSTEM INFORMATION

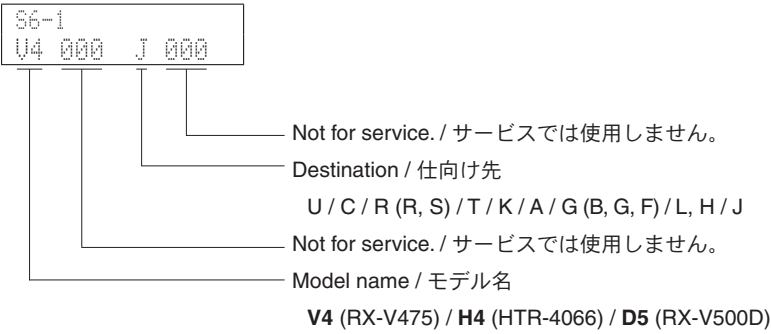
モデル名、仕向け先が表示されます。

S6-1. MODEL

The model name and destination are displayed.

S6-1. MODEL

モデル名、仕向け先が表示されます。



S6-2. VERIFY

Not for service.

S6-2. VERIFY

サービスでは使用しません。



■ POWER AMPLIFIER ADJUSTMENT / パワーアンプ調整

1. Right after power is turned on, confirm that the voltage across the terminals of R2152 (SURROUND Rch), R2149 (FRONT Rch), R2151 (CENTER), R2150 (FRONT Lch) and R2153 (SURROUND Lch) are within the confines of 0.1 mV to 10 mV.
2. If measured voltage exceeds 10 mV, remove R2107 (SURROUND Rch), R2111 (FRONT Rch), R2110 (CENTER), R2109 (FRONT Lch) and R2112 (SURROUND Lch), and then reconfirm the voltage.

Attention

If the measured voltage exceeds 10 mV after repairing the power amplifier, check other parts again for any possible defect before removing the resistor.

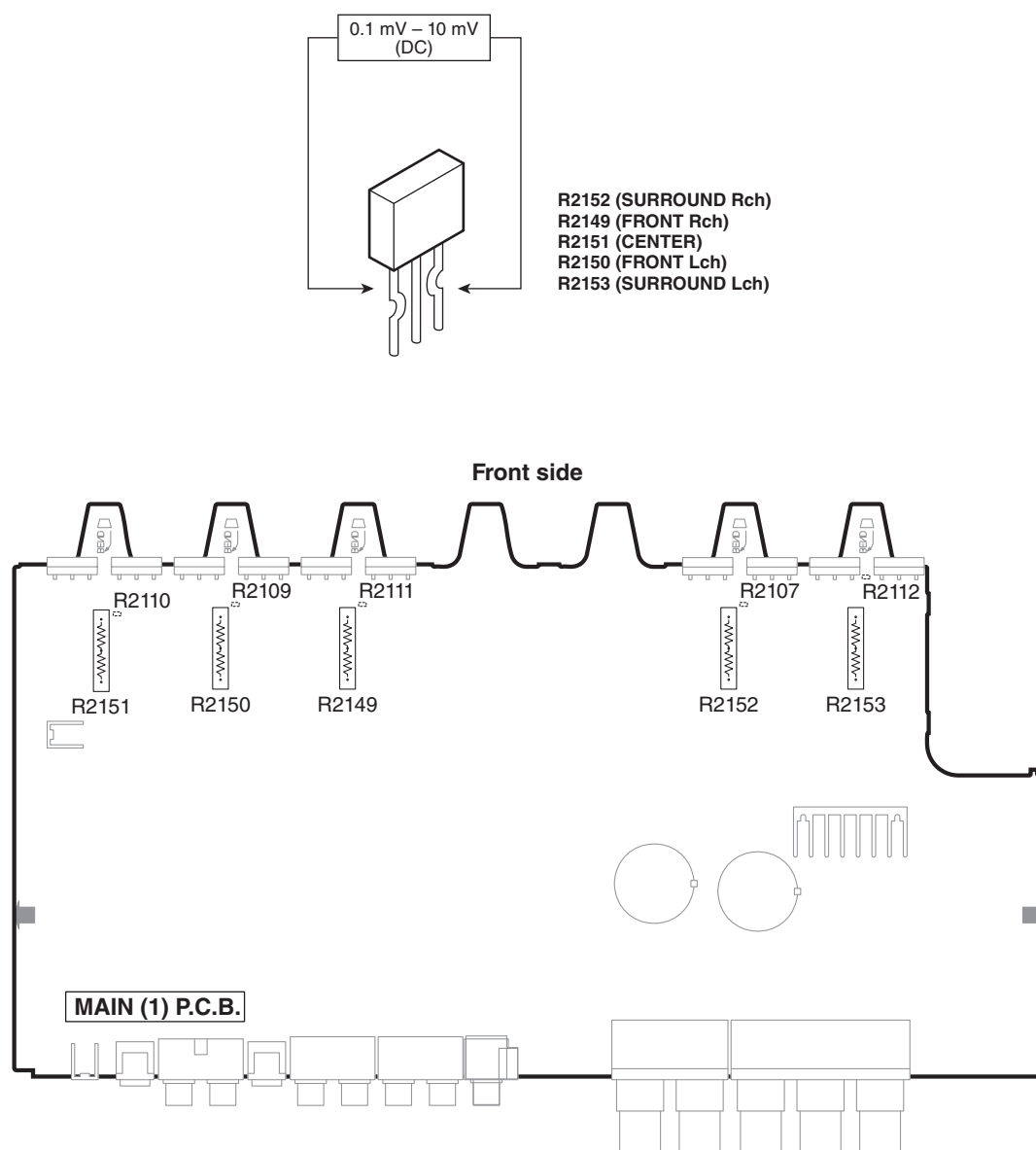
3. Confirm that the voltage is within the confines of 0.2 mV to 15 mV after 60 minutes.

1. 電源投入直後、R2152 (SURROUND Rch)、R2149 (FRONT Rch)、R2151 (CENTER)、R2150 (FRONT Lch)、R2153 (SURROUND Lch) の端子間電圧を測定し、0.1 mV から 10 mV の間であることを確認してください。
2. 電圧が 10 mV を超えている場合は、R2107 (SURROUND Rch)、R2111 (FRONT Rch)、R2110 (CENTER)、R2109 (FRONT Lch)、R2112 (SURROUND Lch) を外し、電圧を再確認してください。

注意

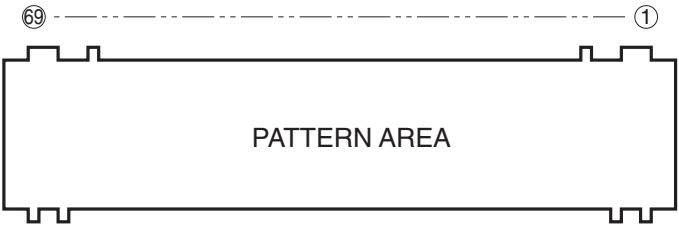
パワーアンプ修理後に 10 mV を超えている場合は、抵抗を外す前に故障箇所を調べてください。

3. 60 分後、電圧が 0.2 mV ～ 15 mV であることを確認してください。



■ DISPLAY DATA

● V4001 : 18-MT-11GNAK (OPERATION P.C.B.)



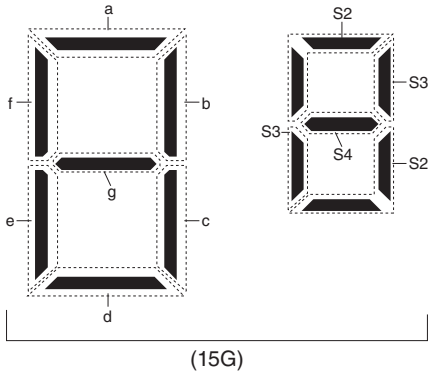
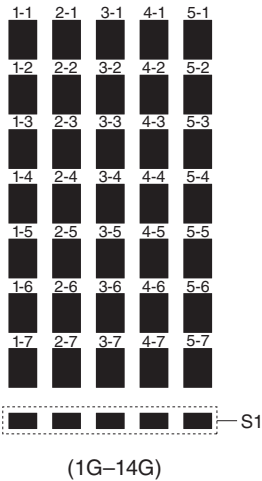
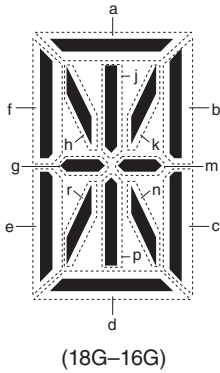
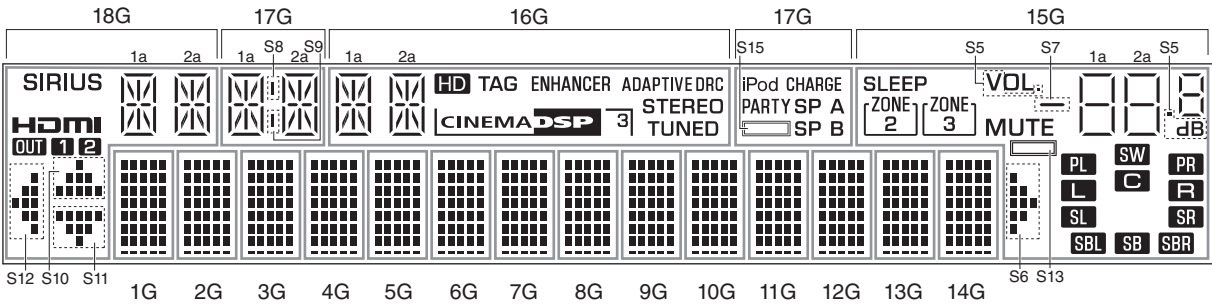
● PIN CONNECTION

Pin No.	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35
Connection	F2	NX	NP	NP	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16	P17	P18	P19	P20	P21	P22	P23	P24	P25	P26	P27	P28	P29	P30	P31

Pin No.	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Connection	P32	P33	P34	P35	P36	NX	NX	NX	NX	NX	NX	NX	18G	17G	16G	15G	14G	13G	12G	11G	10G	9G	8G	7G	6G	5G	4G	3G	2G	1G	NP	NP	NX	F1

Note : 1) F1, F2 Filament pin 2) NP No pin 3) NX No extend pin 4) 1G-18G Grid pin

● GRID ASSIGNMENT



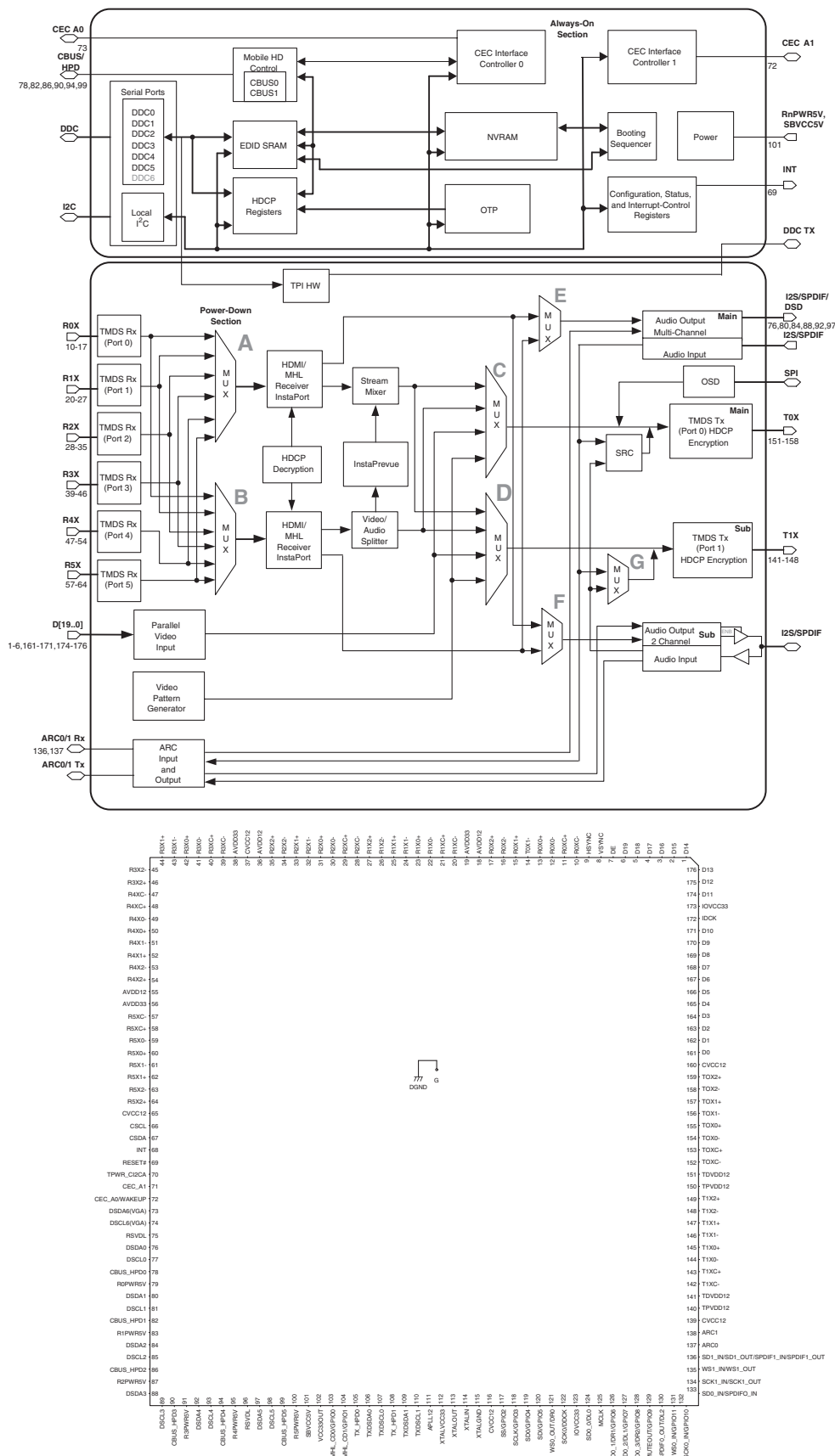
● ANODE CONNECTION

	18G	17G	16G	15G	1G-14G
P1	1a	1a	1a	S5	1-1
P2	1h	1h	1h	S7	2-1
P3	1j	1j	1j	1d	3-1
P4	1k	1k	1k	2d	4-1
P5	1b	1b	1b	S2	5-1
P6	1f	1f	1f	1e	1-2
P7	1m	1m	1m	2e	2-2
P8	1g	1g	1g	S3	3-2
P9	1c	1c	1c	1c	4-2
P10	1e	1e	1e	2c	5-2
P11	1r	1r	1r	S4	1-3
P12	1p	1p	1p	1g	2-3
P13	1n	1n	1n	2g	3-3
P14	1d	1d	1d	1f	4-3
P15	2a	2a	2a	2f	5-3
P16	2h	2h	2h	1b	1-4
P17	2j	2j	2j	2b	2-4
P18	2k	2k	2k	1a	3-4
P19	2b	2b	2b	2a	4-4
P20	2f	2f	2f	PL	5-4
P21	2m	2m	2m	SW	1-5
P22	2g	2g	2g	PR	2-5
P23	2c	2c	2c	L	3-5
P24	2e	2e	2e	C	4-5
P25	2r	2r	2r	R	5-5
P26	2p	2p	2p	SL	1-6
P27	2n	2n	2n	SR	2-6
P28	2d	2d	2d	SBL	3-6
P29	SIRIUS	S8	HD	SB	4-6
P30	OUT	S9	TAG	SBR	5-6
P31	HDMI	iPod CHARGE	CINEMA DSP	S6	1-7
P32	1	SP B	3	S13	2-7
P33	2	S15	STEREO	MUTE	3-7
P34	S12	SP A	TUNED	ZONE 2	4-7
P35	S10	PARTY	ENHANCER	ZONE 3	5-7
P36	S11	—	ADAPTIVE DRC	SLEEP	S1

IC DATA

IC1: SI9573CTUC (DIGITAL P.C.B.)
HDMI port processors

* No replacement part available. / サービス部品供給なし



HDMI Receiver and MHL Port Pins

Pin No.	Function Name	Type	I/O	Detail of Function
12	R0X0-	TMDS	Input	HDMI receiver Port 0 TMDS input data pairs.
13	R0X0+			
14	R0X1-			
15	R0X1+			
16	R0X2-			
17	R0X2+			
10	R0XC-	TMDS	Input	HDMI receiver Port 0 TMDS input clock pair.
11	R0XC+			
22	R1X0-	TMDS	Input	HDMI receiver Port 1 TMDS input data pairs.
23	R1X0+			
24	R1X1-			
25	R1X1+			
26	R1X2-			
27	R1X2+			
20	R1XC-	TMDS	Input	HDMI receiver Port 1 TMDS input clock pair.
21	R1XC+			
30	R2X0-	TMDS	Input	HDMI receiver Port 2 TMDS input data pairs.
31	R2X0+			
32	R2X1-			
33	R2X1+			
34	R2X2-			
35	R2X2+			
28	R2XC-	TMDS	Input	HDMI receiver Port 2 TMDS input clock pair.
29	R2XC+			
41	R3X0-	TMDS	Input	HDMI receiver Port 3 TMDS input data pairs.
42	R3X0+			
43	R3X1-			
44	R3X1+			
45	R3X2-			
46	R3X2+			
39	R3XC-	TMDS	Input	HDMI receiver Port 3 TMDS input clock pair.
40	R3XC+			
49	R4X0-	TMDS	Input	HDMI receiver Port 4 TMDS input data pairs.
50	R4X0+			
51	R4X1-			
52	R4X1+			
53	R4X2-			
54	R4X2+			
47	R4XC-	TMDS	Input	HDMI receiver Port 4 TMDS input clock pair.
48	R4XC+			
59	R5X0-	TMDS	Input	HDMI receiver Port 5 TMDS input data pairs.
60	R5X0+			
61	R5X1-			
62	R5X1+			
63	R5X2-			
64	R5X2+			
57	R5XC-	TMDS	Input	HDMI receiver Port 5 TMDS input clock pair.
58	R5XC+			

Note: For Port 0 and Port 5 that have been configured as MHL inputs, the R0X0+ and R0X0- pin pair and R5X0+ and R5X0- pin pair carry the respective MHL signals.

HDMI Transmitter Port Pins

Pin No.	Function Name	Type	I/O	Detail of Function
154	T0X0-	TMDS	Output	HDMI transmitter Port 0 TMDS output data pairs. Main HDMI transmitter output Port TMDS data pairs.
155	T0X0+			
156	T0X1-			
157	T0X1+			
158	T0X2-			
159	T0X2+			
152	T0XC-	TMDS	Output	HDMI transmitter Port 0 TMDS output clock pair. Main HDMI transmitter output Port TMDS clock pair.
153	T0XC+			
144	T1X0-	TMDS	Output	HDMI transmitter Port 1 TMDS output data pairs. Sub HDMI transmitter output Port TMDS data pairs.
145	T1X0+			
146	T1X1-			
147	T1X1+			
148	T1X2-			
149	T1X2+			
142	T1XC-	TMDS	Output	HDMI transmitter Port 1 TMDS output clock pair. Sub HDMI transmitter output Port TMDS clock pair.
143	T1XC+			

Audio Return Channel Pins

Pin No.	Function Name	Type	I/O	Detail of Function
137	ARC0	Analog	Input/Output	Audio Return Channels 0 and 1. These pins are used to transmit or receive an IEC60958-1 audio stream. In ARC transmitter mode, received on the SPDIFn_IN input pin, this pin transmits an S/PDIF signal to an ARC receiver-capable source (such as HTiB) or a repeater (such as AVR) devices, using single-mode ARC. In ARC receiver mode, transmitted through the SPDIFn_OUT pin, this pin receives an S/PDIF signal from an ARC transmitter-capable sink (such as DTV) device, using single-mode ARC. In combination with external components, common-mode ARC can be received. Each channel can either be an ARC input or an ARC output at one time.
138	ARC1			

Audio Pins

Pin No.	Function Name	Type	I/O	Detail of Function
121	WS0_OUT/DR0	LVTTTL	Output	Main port I2S word select output/DSD data right bit 0.
122	SCK0/DDCK	LVTTTL	Output	Main port I2S serial clock output/DSD clock output.
124	SDO_0/DL0	LVTTTL	Output	Main port I2S serial data 0 output/DSD data left bit 0 output.
125	MCLK	LVTTTL	Output	Master clock output.
126	SDO_1/DR1/GPIO6	LVTTTL	Output	Main port I2S serial data 1 output/DSD data right bit 1 output/programmable GPIO 6.
127	SDO_2/DL1/GPIO7	LVTTTL	Output	Main port I2S serial data 2 output/DSD data left bit 1 output/programmable GPIO 7.
128	SDO_3/DR2/GPIO8	LVTTTL	Output	Main port I2S serial data 3 output/DSD data right bit 2/programmable GPIO 8.
129	MUTEOUT/GPIO9	LVTTTL	Input/Output	Mute audio output/programmable GPIO 9.
130	SPDIF0_OUT/DL2	Analog/LVTTTL	Output	Main port S/PDIF output/DSD data left bit 2.
131	WS0_IN/GPIO11	LVTTTL	Input/Output	Main port I2S word select input/programmable GPIO 11.
132	SCK0_IN/GPIO10	LVTTTL	Input/Output	Main port I2S serial clock input/programmable GPIO 10.
133	SD0_IN/SPDIF0_IN	Analog/LVTTTL	Input	Main port I2S serial data input/S/PDIF input.
134	SCK1_IN/SCK1_OUT	LVTTTL	Input/Output	Sub port I2S serial clock1 input/I2S serial bit clock output.
135	WS1_IN/WS1_OUT	LVTTTL	Input/Output	Sub port I2S word select input/I2S word select output.
136	SD1_IN/SD1_OUT/SPDIF1_IN/SPDIF1_OUT	LVTTTL	Input/Output	Sub port I2S serial data input/I2S serial data1 output/ SPDIF input/SPDIF output.

Crystal Pins

Pin No.	Function Name	Type	I/O	Detail of Function
113	XTALOUT	LVTTTL 5 V tolerant	Output	Crystal clock output.
114	XTALIN	LVTTTL 5 V tolerant	Input	Crystal clock input.

SPI Interface Pins

Pin No.	Function Name	Type	I/O	Detail of Function
117	SS/GPIO2	LVTTTL	Input/Output	SPI slave select/programmable GPIO 2.
118	SCLK/GPIO3	LVTTTL Schmitt Open drain/	Input/Output	SPI clock/programmable GPIO 3.
119	SDO/GPIO4	LVTTTL Schmitt Open drain	Input/Output	SPI slave data output/master data input/programmable GPIO 4.
120	SDI/GPIO5	LVTTTL Schmitt Open drain	Input/Output	SPI slave data input/master data output/programmable GPIO 5.

Parallel Video Bus

Pin No.	Function Name	Type	I/O	Detail of Function
1	D14	LVTTTL	Input	Video data inputs. The video data inputs can be configured to support a wide variety of input formats, including multiple RGB and YCbCr bus formats, using register settings.
2	D15			
3	D16			
4	D17			
5	D18			
6	D19			
161	D0			
162	D1			
163	D2			
164	D3			
165	D4			
166	D5			
167	D6			
168	D7			
169	D8			
170	D9			
171	D10			
174	D11			
175	D12			
176	D13			
7	DE	LVTTTL	Input	Data enable input.
9	HSYNC	LVTTTL	Input	Horizontal sync input.
8	VSYNC	LVTTTL	Input	Vertical sync input.
172	IDCK	LVTTTL	Input	Input data clock.

System Switching Pins

Pin No.	Function Name	Type	I/O	Detail of Function
76	DSDA0	LVTTL Schmitt Open drain 5 V tolerant	Input/Output	DDC I2C data for respective HDMI receiver port. These signals are true open drain, and do not pull to ground when power is not applied to the device. These pins require an external pull-up resistor.
80	DSDA1			
84	DSDA2			
88	DSDA3			
92	DSDA4			
97	DSDA5			
73	DSDA6(VGA)	LVTTL Schmitt Open drain 5 V tolerant	Input/Output	DDC I2C data for VGA port. This signal is true open drain, and does not pull to ground when power is not applied to the device. This pin requires an external pull-up resistor.
77	DSCL0	LVTTL Schmitt Open drain 5 V tolerant	Input	DDC I2C clock for respective HDMI receiver port. These signals are true open drain, and do not pull to ground when power is not applied to the device. These pins require an external pull-up resistor.
81	DSCL1			
85	DSCL2			
89	DSCL3			
93	DSCL4			
98	DSCL5			
74	DSCL6(VGA)	LVTTL Schmitt Open drain 5 V tolerant	Input	DDC I2C clock for VGA port. This signal is true open drain, and does not pull to ground when power is not applied to the device. This pin requires an external pull-up resistor.
106	TXDSDA0	LVTTL Schmitt Open drain 5 V tolerant	Input/Output	DDC master I2C data for HDMI transmitter Port 0. This signal is true open drain, and does not pull to ground when power is not applied to the device. This pin requires an external pull-up resistor.
109	TXDSDA1	LVTTL Schmitt Open drain 5 V tolerant	Input/Output	DDC master I2C data for HDMI transmitter Port 1. This signal is true open drain, and does not pull to ground when power is not applied to the device. This pin requires an external pull-up resistor.
107	TXDSCL0	LVTTL Schmitt Open drain 5 V tolerant	Input/Output	DDC master I2C clock for HDMI transmitter Port 0. This signal is true open drain, and does not pull to ground when power is not applied to the device. This pin requires an external pull-up resistor.
110	TXDSCL1	LVTTL Schmitt Open drain 5 V tolerant	Input/Output	DDC master I2C clock for HDMI transmitter Port 1. This signal is true open drain, and does not pull to ground when power is not applied to the device. This pin requires an external pull-up resistor.
79	R0PWR5V	Power	Input	5 V port detection input for respective HDMI receiver port. Connect to 5 V signal from HDMI input connector. These pins require a 10 ohms series resistor, a 5.1 k-ohms pull down resistor, and at least a 1 μ F capacitor to ground.
83	R1PWR5V			
87	R2PWR5V			
91	R3PWR5V			
95	R4PWR5V			
100	R5PWR5V			
78	CBUS_HPD0	LVTTL 1.5 mA 5 V tolerant Analog	Input/Output	Hot plug detect output for the respective HDMI receiver port. In MHL mode, these pins serve as the respective CTRL bus.
82	CBUS_HPD1			
86	CBUS_HPD2			
90	CBUS_HPD3			
94	CBUS_HPD4			
99	CBUS_HPD5			
105	TX_HPD0	LVTTL 5 V tolerant	Input	Hot plug detect input for HDMI transmitter Port 0.
108	TX_HPD1	LVTTL 5 V tolerant	Input	Hot plug detect input for HDMI transmitter Port 1.
103	MHL_CD0/GPIO0	LVTTL	Input/Output	MHL cable detect 0/programmable GPIO 0.
104	MHL_CD1/GPIO1	LVTTL	Input/Output	MHL cable detect 1/programmable GPIO 1.

Control Pins

Pin No.	Function Name	Type	I/O	Detail of Function
66	CSCL	Schmitt Open drain 5 V tolerant	Input	Local configuration/status I2C clock. Chip configuration/status is accessed via this I2C port. This pin is true open drain, so it does not pull to ground if power is not applied.
67	CSDA	LVTTL Schmitt Open drain 5 V tolerant	Input/Output	Local configuration/status I2C data. Chip configuration/status is accessed via this I2C port. This pin is true open drain, so it does not pull to ground if power is not applied.
69	RESET#	Schmitt	Input	External reset. Active LOW. Must be pulled up to VCC33OUT. When main power is not provided to the system, the microprocessor must present a high impedance of at least 100 k-ohms to RESET#. If this condition is not met, a circuit to block the leakage from VCC33OUT to the microprocessor GPIO may be required.

Configuration Pins

Pin No.	Function Name	Type	I/O	Detail of Function
70	TPWR_C12CA	LVTTL	Input/Output	I2C slave address input / Transmit power sense output. During power-on-reset (POR), this pin is used as an input to latch the I2C subaddress. The level on this pin is latched when the POR transitions from the asserted state to the de-asserted state. After completion of POR, this pin is used as the TPWR output. A register setting can change this pin to show if the active port is receiving a TMDS clock.
68	INT	Schmitt Open drain 8 mA 3.3 V tolerant	Output	Interrupt output. This is an open-drain output and requires an external pull-up resistor.

CEC Pins

Pin No.	Function Name	Type	I/O	Detail of Function
72	CEC_A0	CEC Compliant 5V tolerant, Schmitt triggered, LVTTL	Input/Output	Primary CEC I/O used for interfacing to CEC devices This signal is electrically compliant with the CEC specification. As an input, this pin acts as an LVTTL schmitt triggered input and is 5 V tolerant. As an output, the pin acts as an NMOS driver with resistive pull-up. This pin has an internal pull-up resistor. This signal should be connected to the CEC signal of all HDMI input and output ports if the system supports just one CEC line. OR In a system designed to have separate CEC connectivity for the HDMI input and output ports, this signal should be connected to the CEC signal of all the input ports supported in the system. This signal and CEC_A0 each connect to a separate CEC controller within the port processor and are independent of each other.
71	CEC_A1	CEC Compliant 5V tolerant, Schmitt triggered, LVTTL	Input/Output	Secondary CEC I/O used for interfacing to CEC devices. This signal is electrically compliant with the CEC specification. As an input, this pin acts as an LVTTL schmitt triggered input and is 5 V tolerant. As an output, the pin acts as an NMOS driver with resistive pull-up. This pin has an internal pull-up resistor. This is an optional CEC signal provided for system designers who want to implement a system with two independent CEC lines, such as a system that supports a separate CEC line for the HDMI input ports and the HDMI output ports. In the example of a DTV that provides a second HDMI output using the SiI957n port processor; this signal can be connected to the CEC signal of the output port while the CEC_A1 signal is connected to the CEC signal of the input ports. This signal and CEC_A1 each connect to a separate CEC controller within the port processor and are independent of each other.

Power and Ground Pins

Pin No.	Function Name	Type	I/O	Detail of Function
19	AVDD33	Power	3.3 V	TMDS core VDD.
38				
56				
123	IOVCC33	Power	3.3 V	I/O VCC.
173				
101	SBVCC5	Power	5.0 V	Local power from system. This pin requires a 10 ohms series resistor.
18	AVDD13	Power	1.3 V	TMDS receiver core VDD.
36				
55				
37	CVCC13	Power	1.3 V	Digital core VCC.
65				
116				
139				
160				
111	APLL13	Power	1.3 V	PLL analog VCC.
102	VCC33OUT	Power	3.3 V	Internal regulator 3.3 V output.
140	TPVDD13	Power	1.3 V	Analog power for TMDS Tx core.
150				
141	TDVDD13	Power	1.3 V	Digital power for TMDS Tx core.
151				
112	XTALVCC33	Power	3.3 V	PLL crystal oscillator power.
115	XTALGND	Ground	GND	PLL crystal oscillator ground.
ePad	GND	Ground	GND	The ePad must be soldered to ground, as this is the only ground connection for the device.

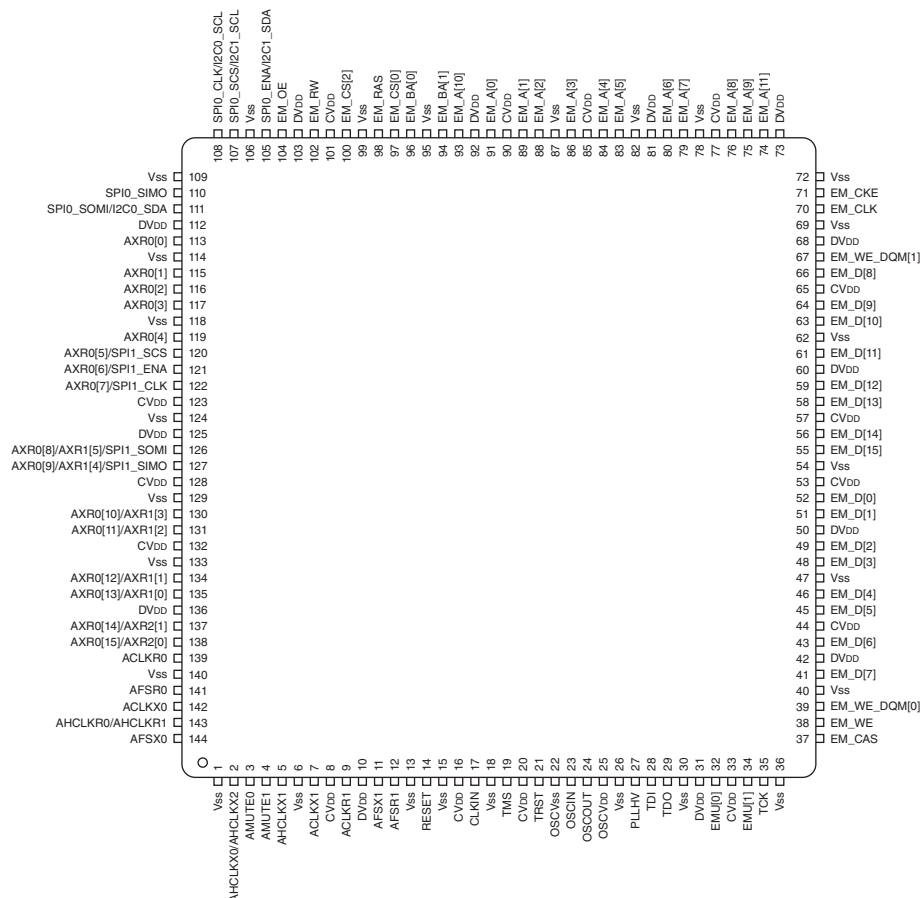
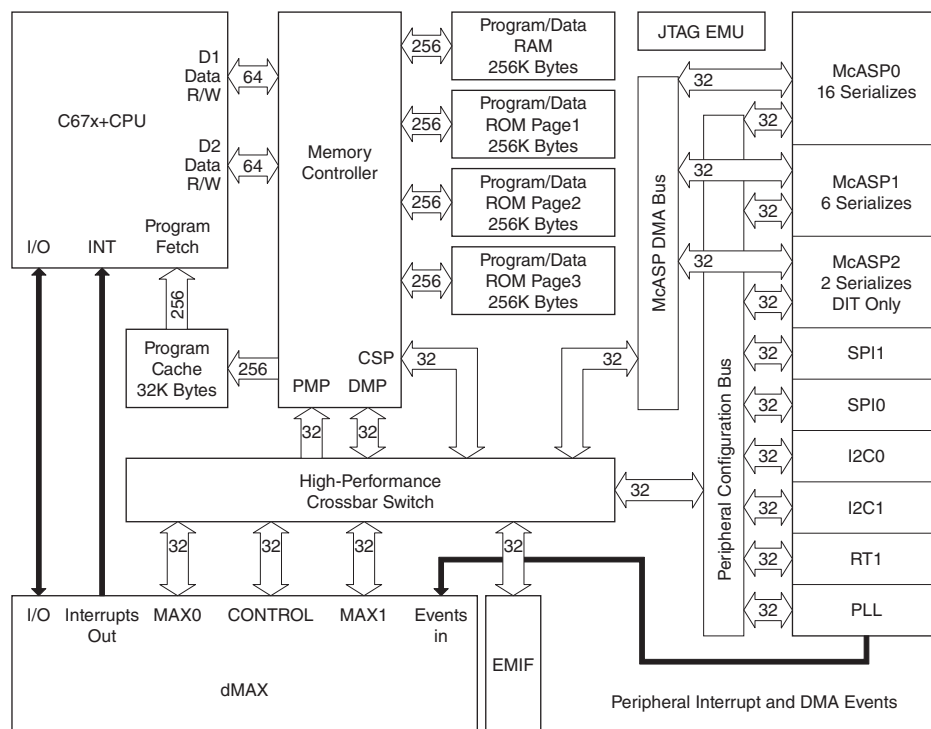
Reserved Pin

Pin No.	Function Name	Type	Detail of Function
75	RSVDL	Reserved	Reserved, must be tied to ground.
96			

IC41: D70YE101BRFP266 (DIGITAL P.C.B.)

Decoder/Post processor

* No replacement part available./ サービス部品供給なし



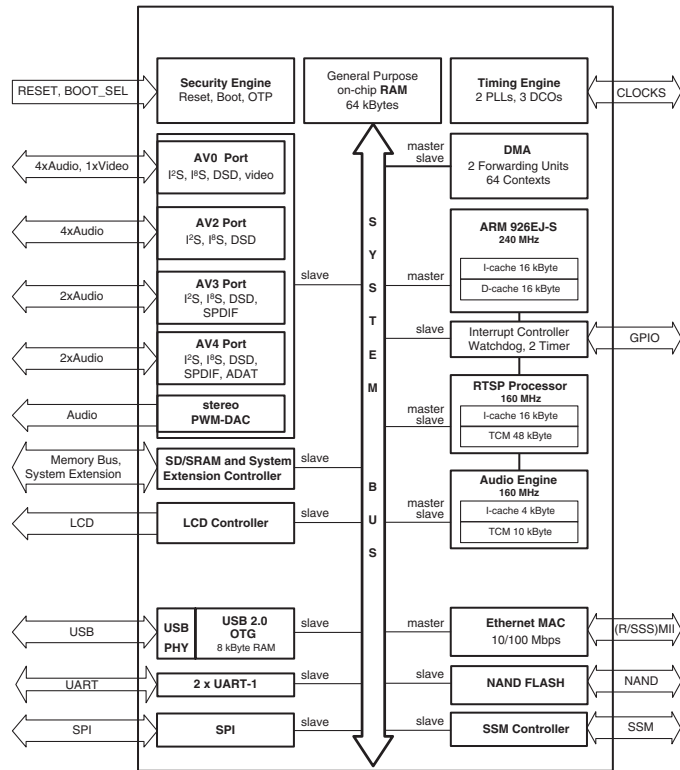
No.	Function Name (P.C.B.)	I/O	Detail of Function
1	VSS		
2	AHCLKX0/AHCLKX2	IO	McASP0 and McASP2 transmit master clock
3	AMUTE0	IO	McASP0 mute output
4	AMUTE1	IO	McASP1 mute output
5	AHCLKX1	IO	McASP1 transmit master clock
6	VSS		
7	ACLKX1	IO	McASP1 transmit bit clock
8	CVDD		
9	ACLKR1	IO	McASP1 receive bit clock
10	DVDD		
11	AFSX1	IO	McASP1 transmit frame Sync (L/R clock)
12	AFSR1	IO	McASP1 receive frame Sync (L/R clock)
13	VSS		
14	RESET	IO	Device reset pin
15	VSS		
16	CVDD		
17	CLKIN	IO	Alternate clock input (3.3-V LVCMOS input)
18	VSS		
19	TMS	IO	Test mode select
20	CVDD		
21	TRST	IO	Test reset
22	OSCVSS	PWR	Oscillator Vss tap point (for filter only)
23	OSCIN	IO	1.2-V oscillator input
24	NC	O	
25	OSCVDD	PWR	Oscillator 1.2-V Vpp tap point (for filter only)
26	VSS		
27	PLLHV	PWR	PLL 3.3-V supply input (requires external filter)
28	TDI	IO	Test data in
29	TDO	OZ	Test data out
30	VSS		
31	DVDD		
32	EMU[0]	IO	Emulation pin 0
33	CVDD		
34	EMU[1]	IO	Emulation pin 1
35	TCK	IO	Test clock
36	Ground(Vss)		
37	EM_CAS	O	SDRAM column address strobe
38	EM_WE	O	SDRAM write enable
39	EM_WE_DQM[0]	O	Write enable or byte enable for EM_D [7:0]
40	VSS		
41	EM_D[7]	IO	EMIF data bus [lower 16-bits]
42	DVDD		
43	EM_D[6]	IO	EMIF data bus [lower 16-bits]
44	CVDD		
45	EM_D[5]	IO	EMIF data bus [lower 16-bits]
46	EM_D[4]	IO	EMIF data bus [lower 16-bits]
47	VSS		
48	EM_D[3]	IO	EMIF data bus [lower 16-bits]
49	EM_D[2]	IO	EMIF data bus [lower 16-bits]
50	DVDD		

No.	Function Name (P.C.B.)	I/O	Detail of Function
51	EM_D[1]	IO	EMIF data bus [lower 16-bits]
52	EM_D[0]	IO	EMIF data bus [lower 16-bits]
53	CVDD		
54	VSS		
55	EM_D[15]	IO	EMIF data bus [lower 16-bits]
56	EM_D[14]	IO	EMIF data bus [lower 16-Bits]
57	CVDD		
58	EM_D[13]	IO	EMIF data bus [lower 16-Bits]
59	EM_D[12]	IO	EMIF data bus [lower 16-Bits]
60	DVDD		
61	EM_D[11]	IO	EMIF data bus [lower 16-Bits]
62	VSS		
63	EM_D[10]	IO	EMIF data bus [lower 16-Bits]
64	EM_D[9]	IO	EMIF data bus [lower 16-Bits]
65	CVDD		
66	EM_D[8]	IO	EMIF data bus [lower 16-bits]
67	EM_WE_DQM[1]	O	Write enable or byte enable for EM_D [15:8]
68	DVDD		
69	VSS		
70	EM_CLK	O	SDRAM clock
71	EM_CKE	O	SDRAM clock enable
72	VSS		
73	DVDD		
74	EM_A[11]	O	EMIF address bus
75	EM_A[9]	O	EMIF address bus
76	EM_A[8]	O	EMIF address bus
77	CVDD		
78	VSS		
79	EM_A[7]	O	EMIF address bus
80	EM_A[6]	O	EMIF address bus
81	DVDD		
82	VSS		
83	EM_A[5]	O	EMIF address bus
84	EM_A[4]	O	EMIF address bus
85	CVDD		
86	EM_A[3]	O	EMIF address bus
87	VSS		
88	EM_A[2]	O	EMIF address bus
89	EM_A[1]	O	EMIF address bus
90	CVDD		
91	EM_A[0]	O	EMIF address bus
92	DVDD		
93	EM_A[10]	O	EMIF address bus
94	EM_BA[1]	O	SDRAM bank address and asynchronous memory Low-Order address
95	VSS		
96	EM_BA[0]	O	SDRAM bank address and asynchronous memory Low-Order address
97	EM_CS[0]	O	SDRAM chip select
98	EM_RAS	O	SDRAM row address strobe
99	VSS		
100	EM_CS[2]	O	Asynchronous memory chip select

No.	Function Name (P.C.B.)	I/O	Detail of Function
101	CVDD		
102	NC	O	Asynchronous memory read/not write
103	DVDD		
104	EM_OE	O	SDRAM output enable
105	SPI0_ENA/I2C1_SDA	IO	SPI0 enable (ready) or I2c1 serial data
106	VSS		
107	SPI0_ENA/I2C1_SCL	IO	SPI0 enable (ready) or I2c1 serial clock
108	SPI0_CLK/I2C0_SCL	IO	SPI0 serial clock or I2c0 serial clock
109	VSS		
110	SPI0_SIMO	IO	SPI0 data pin slave in master out
111	SPI0_SOMI/I2C0_SDA	IO	SPI0 data pin slave out master in or I2C0 serial data
112	DVDD		
113	AXR0[0]	IO	McASP0 serial data 0
114	VSS		
115	AXR0[1]	IO	McASP0 serial data 1
116	AXR0[2]	IO	McASP0 serial data 2
117	AXR0[3]	IO	McASP0 serial data 3
118	VSS		
119	AXR0[4]	IO	McASP0 serial data 4
120	SPI1_SCS	IO	McASP0 serial data 5 or SPI1 slave chip select
121	SPI1_ENA	IO	McASP0 serial data 6 or SPI1 enable (ready)
122	SPI1_CLK	IO	McASP0 serial data 7 or SPI1 serial clock
123	CVDD		
124	VSS		
125	DVDD		
126	/SPI1_SOMI	IO	McASP0 serial data 8 or McASP1 serial data 5 or SPI1 data pin slave out master in
127	/SPI1_SIMO	IO	McASP0 serial data 9 or McASP1 serial data 4 or SPI1 data pin slave in master out
128	CVDD		
129	VSS		
130	AXR0[10]	IO	McASP0 serial data 10 or McASP1 serial data 3
131	AXR0[11]	IO	McASP0 serial data 11 or McASP1 serial data 2
132	CVDD		
133	VSS		
134	AXR0[12]	IO	McASP0 serial data 12 or McASP1 serial data 1
135	AXR0[13]	IO	McASP0 serial data 13 or McASP1 serial data 0
136	DVDD		
137	AXR0[14]	IO	McASP0 serial data 14 or McASP2 serial data 1
138	AXR0[15]	IO	McASP0 serial data 15 or McASP2 serial data 0
139	ACLKR0	IO	McASP0 receive bit clock
140	VSS		
141	AFSR0	IO	McASP0 receive frame Sync (L/R clock)
142	ACLKX0	IO	McASP0 transmit bit clock
143	AHCLKR0/AHCLKR1	IO	McASP0 and McASP1 receive master clock
144	AFSX0	IO	McASP0 transmit frame Sync (L/R clock)

IC951: DM860A (DIGITAL P.C.B.)
Network microprocessor

* No replacement part available. / サービス部品供給なし



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	USBDN	VDD33 USBC	VSS33 USBC	n.c.	n.c.	VDD33	RFCLKP	RFRXQP	RFRXIP	HIGHZ	SSMD0	SSMD4	SSMCMD	RXD1	TDO	TDI	A0	A1	A
B	USBDP	VDD33 USBT	VSS33 USBT	n.c.	n.c.	VSS	RFCLKN	RFRXQN	RFRXIN	TEST1	SSMD1	SSMD5	TXD1	RXD0	TMS	SPICLK	SPINCS1	A2	B
C	VSS12 USB	USBREXT	USBXO	USBXI	NRES12 OUT	VSS	RREF	n.c.	n.c.	SSMCLK	SSMD2	SSMD6	TXD0	TCK	SPINCS0	A3	A4	A5	C
D	VDD12 USB	USBVBUS	USBATST	NRES33 OUT	NRES33 REF	VDD33	VDD12	SSMWP	SSMCP	SSMD3	SSMD7	NRESET	SPDI	SPIDO	A6	A7	A8	A8	D
E	VSS33 RTC	USBDI	USBVB USDRV	NC		VDD12 CORE	VDD12 CORE	VDD33IO	VDD33IO	VDD12 CORE	VDD12 CORE	VDD33IO	VDD33IO		A9	A10	A11	A12	E
F	VDD33 RTC	RTCXIN	VDD33 PLL	NC	VDD33IO	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD12 CORE	A13_RAS	A14_CAS	A15_BA0	A16_BA1	F
G	VDD12 DCO	RTXCOUT	VSS33 PLL	NC	VDD33IO	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD12 CORE	A17_DQ M0	A18_DQ M1	A19	A20	G
H	VSS12 DCO	VSS12 PLL	VDD12 PLL	NC	VDD12 CORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33IO	A21	A22	A23	NCS3	H
J	PDOUT1	VCO1	XTALO	NC	VDD12 CORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33IO	NCS0	NCS1	NCS2	MEMCKE	J
K	PDOUT0	VCO0	XTALI	AOUTLP	VDD33IO	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD12 CORE	MEMCLK	NWE	NOE	NWAIT	K
L	AV0CLK	AOUTLN	AOUTRN	AOUTRP	VDD33IO	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD12 CORE	D3	D2	D1	D0	L
M	AV0 CTRL0	AV0 CTRL1	AV0 CTRL2	AV0 DATA3	VDD12 CORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33IO	D7	D6	D5	D4	M
N	AV0 DATA2	AV0 DATA1	AV0 DATA0	AV1 DATA3	VDD12 CORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD33IO	D11	D10	D9	D8	N
P	AV1 DATA2	AV1 DATA1	AV1 DATA0	AV2 DATA3		VDD33IO	VDD33IO	VDD12 CORE	VDD12 CORE	VDD33IO	VDD33IO	VDD12 CORE	VDD12 CORE		FD0	FD1	D13	D12	P
R	AV2CLK	AV2 CTRL1	AV2 CTRL2	AV3CLK	AV3 DATA1	LCDD11	LCDD7	LCDD3	LCD CTRL0	VPP	MIITXEN	MIITXCLK	MIIRXER	MIICRS	FD2	FD3	FD4	D14	R
T	AV2 CTRL0	AV2 DATA1	AV3 CTRL1	AV3 DATA0	LCDD14	LCDD10	LCDD6	LCDD2	LCD CTRL1	LCDCLK	MIITXER	MIIRXCLK	MIICOL	MII RXDV	FD5	FD6	FD7	D15	T
U	AV2 DATA2	AV3 CTRL0	AV4 DATA1	LCDD16	LCDD13	LCDD9	LCDD5	LCDD1	LCD CTRL2	MIITXD0	MIITXD2	MIIRXD0	MIIRXD2	MIIMDIO	NFCE0	FCLE	NFWE	NFRB	U
V	NC	AV4 DATA0	LCDD17	LCDD15	LCDD12	LCDD8	LCDD4	LCDD0	LCD CTRL3	MIITXD1	MIITXD3	MIIRXD1	MIIRXD3	MIIMDC	MII PHY CLK	NFWP	NFRE	FALE	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

AV-Port 0

Pin No.	Function Name	I/O	Detail of Function
M4	AV0DATA[3:0]	I/O	Audio/video data. Several formats are supported.
N1			
N2			
N3			
N4	AV1DATA[3:0]	I/O	Video data, together with AV0DATA[3:0]: AV0DATA[3:0] = video[3:0] AV1DATA[3:0] = video[7:4]
P1			
P2			
P3			
L1	AV0CLK	I/O	Data clock. Depending on the AV-Port 0 configuration, this clock is a bit- or byte-clock which is used to transmit or receive the AV0DATA[*] synchronously.
M1	AV0CTRL0	I/O	Configurable sync signal: • Serial audio formats: LRCK input or output. • Video formats: PSYNC input or output.
M2	AV0CTRL1	I/O	Configurable sync signal: • Serial audio formats: Master clock output. • Video formats: DVALID input or output.
M3	AV0CTRL2	I/O	Configurable sync signal: • Video formats: FSYNC input or output.

AV-Port 2

Pin No.	Function Name	I/O	Detail of Function
P4	AV2DATA[3:0]	I/O	Audio data. Several formats are supported.
R3			
T2			
U1			
R1	AV2CLK	I/O	Data clock. Depending on the AV-Port 2 configuration this clock is a bit-clock which is used to transmit or receive the AV2DATA[*] synchronously.
T1	AV2CTRL0	I/O	Configurable sync signal: Serial audio formats: LRCK input or output.
R2	AV2CTRL1	I/O	Configurable sync signal: Serial audio formats: Master clock output.

AV-Port 3

Pin No.	Function Name	I/O	Detail of Function
R5	AV3DATA[1:0]	I/O	Audio data. Several formats are supported.
T4			
R4	AV3CLK	I/O	Data clock. Depending on the AV-Port 3 configuration this clock is a bit-clock which is used to transmit or receive the AV3DATA[*] synchronously.
U2	AV3CTRL0	I/O	Configurable sync signal: Serial audio formats: LRCK input or output.
T3	AV3CTRL1	I/O	Configurable sync signal: Serial audio formats: Master clock output.

AV-Port 4

Pin No.	Function Name	I/O	Detail of Function
U3	AV4DATA[1:0]	I/O	Audio data. Several formats are supported.
V2			

PWM-DAC

Pin No.	Function Name	I/O	Detail of Function
K4	AOUTLP	O	Left channel PWM output (positive).
L2	AOUTLN	O	Left channel PWM output (negative).
L4	AOUTRP	O	Right channel PWM output (positive).
L3	AOUTRN	O	Right channel PWM output (negative).

UART Interface

Pin No.	Function Name	I/O	Detail of Function
B14	RXD0	I	UART-0 receive signal.
C13	TXD0	O	UART-0 transmit signal.
A14	RXD1	I	UART-1 receive signal.
B13	TXD1	O	UART-1 transmit signal.

Serial Peripheral Interface (SPI)

Pin No.	Function Name	I/O	Detail of Function
D14	SPIDIN	I	SPI data receive.
D15	SPIDOUT	O	SPI data transmit.
B16	SPICLK	I/O	SPI clock.
C15	SPINCS0	I/O	Multi-master mode: Chip-select input (used to detect bus conflict). Master only mode: Chip-select 1 output. Slave mode: Chip-select input.
B17	SPINCS1	I/O	Multi-master mode: Chip-select 2 output. Master only mode: Chip-select 2 output. Slave mode: Not used.

External Memory Interface

Pin No.	Function Name	I/O	Detail of Function
T18	D[15:0]	I/O	Data bus for external memory and peripheral access.
R18			
P17			
P18			
N15			
N16			
N17			
N18			
M15			
M16			
M17			
M18			
L15			
L16			
L17			
L18			
E18	A[12:0]	O	Address bus for external memory and peripheral access.
E17			
E16			
E15			
D18			
D17			
D16			
C18			
C17			
C16			
B18			
A18			
A17			
F15	A13_RAS	O	SRAM: Address output SDRAM: Row access strobe
F16	A14_CAS	O	SRAM: Address output SDRAM: Column access strobe
F17	A15_BA0	O	SRAM: Address output SDRAM: Bank select
F18	A16_BA1	O	SRAM: Address output SDRAM: Bank select
G15	A17_DQM0	O	SRAM: Address output SDRAM: Data mask
G16	A18_DQM1	O	SRAM: Address output SDRAM: Data mask
H17	A[23:19]	O	Address bus for external memory and peripheral access.
H16			
H15			
G18			
G17			

Pin No.	Function Name	I/O	Detail of Function
H18	NCS[3:0]	O	Chip select signals. The active memory range for NCS[n] (active low) can be configured. • NCS[0] supports SRAM, can be used for booting. • NCS[1] supports SDRAM or SRAM. • NCS[2] supports SRAM. • NCS[3] supports SRAM.
J17			
J16			
J15			
K17	NOE	O	Output enable, asserted (low) for read operations.
K16	NWE	O	Write enable, asserted (low) for write operations.
K18	NWAIT	I	External wait line. If NWAIT is asserted, memory access will be stalled. Can be configured as either low-active (default) or high-active.
K15	MEMCLK	O	SDRAM system clock.
J18	MEMCKE	O	SDRAM clock enable.

NAND-Flash Interface

Pin No.	Function Name	I/O	Detail of Function
T17	FD[7:0]	I/O	Bi-directional data bus.
T16			
T15			
R17			
R16			
R15			
P16			
P15			
V18	FALE	O	Address latch enable; pull-up/down defines boot mode.
U16	FCLE	O	Command latch enable; pull-up/down defines boot mode.
U15	NFCE0	O	Chip-enable, low-active.
U18	NFRB	I	Ready/busy. NAND flash is busy when NFRB is low.
V17	NFRE	O	Read enable, low-active.
U17	NFWE	O	Write enable, low-active.
V16	NFWP	O	Write protect, low-active.

Ethernet MAC-Phy Interface (MII)

Pin No.	Function Name	I/O	MII	RMII	SMII
U14	MIIDIO	I/O	Management data	Management data	
V14	MIIMDC	O	Management clock	Management clock	
V13	MIIRXD[3]	I	RxD 3	RxD 1	
U13	MIIRXD[2]	I	RxD 2	RxD 0	
V12	MIIRXD[1]	I	RxD 1		Rx-Sync
U12	MIIRXD[0]	I	RxD 0		RxD
T12	MIIRXCLK	I	Receive clock		Receive clock
R13	MIIRXER	I	Receive error	Receive error	
T14	MIIRXDV	I	Receive data valid	Carrier sense/data valid	
V11	MIITXD[3]	O	TxD 3	TxD 1	
U11	MIITXD[2]	O	TxD 2	TxD 0	
V10	MIITXD[1]	O	TxD 1		Tx-Sync
U10	MIITXD[0]	O	TxD 0		TxD
R12	MIITXCLK	I	Transmit clock		Transmit clock
T11	MIITXER	O	Transmit error		
R11	MIITXEN	O	Transmit data enable	Transmit data enable	
T13	MIICOL	I	MII ethernet collision		
R14	MIICRS	I	MII carrier sense		
V15	MIIPHYCLK	O	25.000 MHz clock	50.000 MHz clock	125.000 MHz clock

USB 2.0 OTG

Pin No.	Function Name	I/O	Detail of Function
B1	USBD+	I/O	Positive data line that is connected to the serial USB cable.
A1	USBD-	I/O	Negative data line that is connected to the serial USB cable.
E2	USBID	I	USB ID pin of mini-AB receptacle.
C2	USBREXT	I	External bias resistor (2K7, 1%); connect resistor to VSSUSB.
D2	USBVBUS	I	VBUS voltage sense.
E3	USBVBUSDRV	O	Control signal to control VBUS 5V voltage source.
C4	USBXTALI	I	Oscillator circuit input for a 24.000 MHz crystal (optional). Without external crystal, pull this pin to GND.
C3	USBXTALO	O	Oscillator circuit output for a 24.000 MHz crystal (optional). Without external crystal, leave this pin open.
D3	USBATST	-	Do not connect.

Power-on Reset Pins

Pin No.	Function Name	I/O	Detail of Function
D6	NRES12REF	I	Voltage reference input. NRES12OUT is release when this input voltage exceeds VTH12.
C5	NRES12OUT	O	Open-drain reset (active low) for 1.2V core power supply.
D5	NRES33REF	I	Voltage reference input. NRES33OUT is release when this input voltage exceeds VTH33.
D4	NRES33OUT	O	Open-drain reset (active low) for 3.3V core power supply

Real-Time Clock (RTC) Pins (RTC is Not Supported)

Pin No.	Function Name	I/O	Detail of Function
F2	RTCXIN	I	No connection. Leave this pin open circuit.
G2	RTCXOUT	O	No connection. Leave this pin open circuit.
F1	VDD33RTC	Power	No connection. Leave this pin open circuit.
E1	VSS33RTC	Power	Ground (0 V) for RTC

LCD Interface

Pin No.	Function Name	I/O	TFT Mode	LCD STN monochr.	LCD STN monochr. (double)	LCD STN color	LCD STN color (bias)
V3	LCDD[17]	O	RED5				
U4	LCDD[16]	O	RED4				
V4	LCDD[15]	O	RED3				
T5	LCDD[14]	O	RED2				
U5	LCDD[13]	O	RED1				
V5	LCDD[12]	O	(RED0)				
R6	LCDD[11]	O	GREEN5				
T6	LCDD[10]	O	GREEN4				
U6	LCDD[9]	O	GREEN3				
V6	LCDD[8]	O	GREEN2				
R7	LCDD[7]	O	GREEN1		DATAHIGH3	DATA7	DATA7
T7	LCDD[6]	O	GREEN0		DATAHIGH2	DATA6	DATA6
U7	LCDD[5]	O	BLUE5		DATAHIGH1	DATA5	DATA5
V7	LCDD[4]	O	BLUE4		DATAHIGH0	DATA4	DATA4
R8	LCDD[3]	O	BLUE3	DATA3	DATALOW3	DATA3	DATA3
T8	LCDD[2]	O	BLUE2	DATA2	DATALOW2	DATA2	DATA2
U8	LCDD[1]	O	BLUE1	DATA1	DATALOW1	DATA1	DATA1
V8	LCDD[0]	O	(BLUE0)	DATA0	DATALOW0	DATA0	DATA0
T10	LCDCCLK	O	Byte clock	CL2	CL2	CL2	CL2
V9	LCDCCTRL[3]	O	Display off	Display off	Display off	Display off	Display off
U9	LCDCCTRL[2]	O	Vsync	FLM	FLM	FLM	FLM
T9	LCDCCTRL[1]	O	HSync	CL1	CL1	CL1	CL1
R9	LCDCCTRL[0]	O	DVALID			M/Bias	

SSM Interface

Pin No.	Function Name	I/O	Detail of Function
D12	SSMD[7:0]	I/O	Data lines.
C12			
B12			
A12			
D11			
C11			
B11			
A11			
C10	SSMCLK	O	Clock output.
A13	SSMCMD	O	Command output.
D10	SSMCP	I	Card power input (high = off).
D9	SSMWP	I	Write protect input (low = protect).

External PLL Pins

Pin No.	Function Name	I/O	Detail of Function
J2	VCO[1:0]	I	External oscillator inputs, typically coming from an external VCO. Together with the external loop-filter and the internal clock dividers, each PDOUT/VCO pair can form a complete PLL.
K2			
J1	PDOUT[1:0]	O	Phase discriminator outputs. These signals are charge-pump type outputs. Each of them can be used to feed the loop-filter of a PLL structure.
K1			

Global Pins

Pin No.	Function Name	I/O	Detail of Function
D13	NRESET	I	Reset (active low). When asserted, the chip is placed in the reset state and the peripheral pins are configured as inputs. After deassertion of NRESET, the chip is clocked by XTALI and starts booting from the port configured by the FCLE, FALE pins. The NRESET signal must be asserted after power-up.
K3	XTALI	I	Oscillator circuit input. Internal system clock will be derived from XTALI (internal clock multiplier).
J3	XTALO	O	Oscillator circuit output.
C7	RREF	I	Reference current. Connect a 3.0 k-ohms $\pm 1\%$ resistor to GND.
B10	TEST1	I	Reserved. Connect to VDD for normal operation.
A10	HIGHZ	I	Reserved. Connect to VDD for normal operation.
E4	n.c.	—	Pins must be left unconnected (18x).
F4			
G4			
H4			
J4			
V1			
A4			
A5			
B4			
B5			
C8			
C9			

JTAG Interface

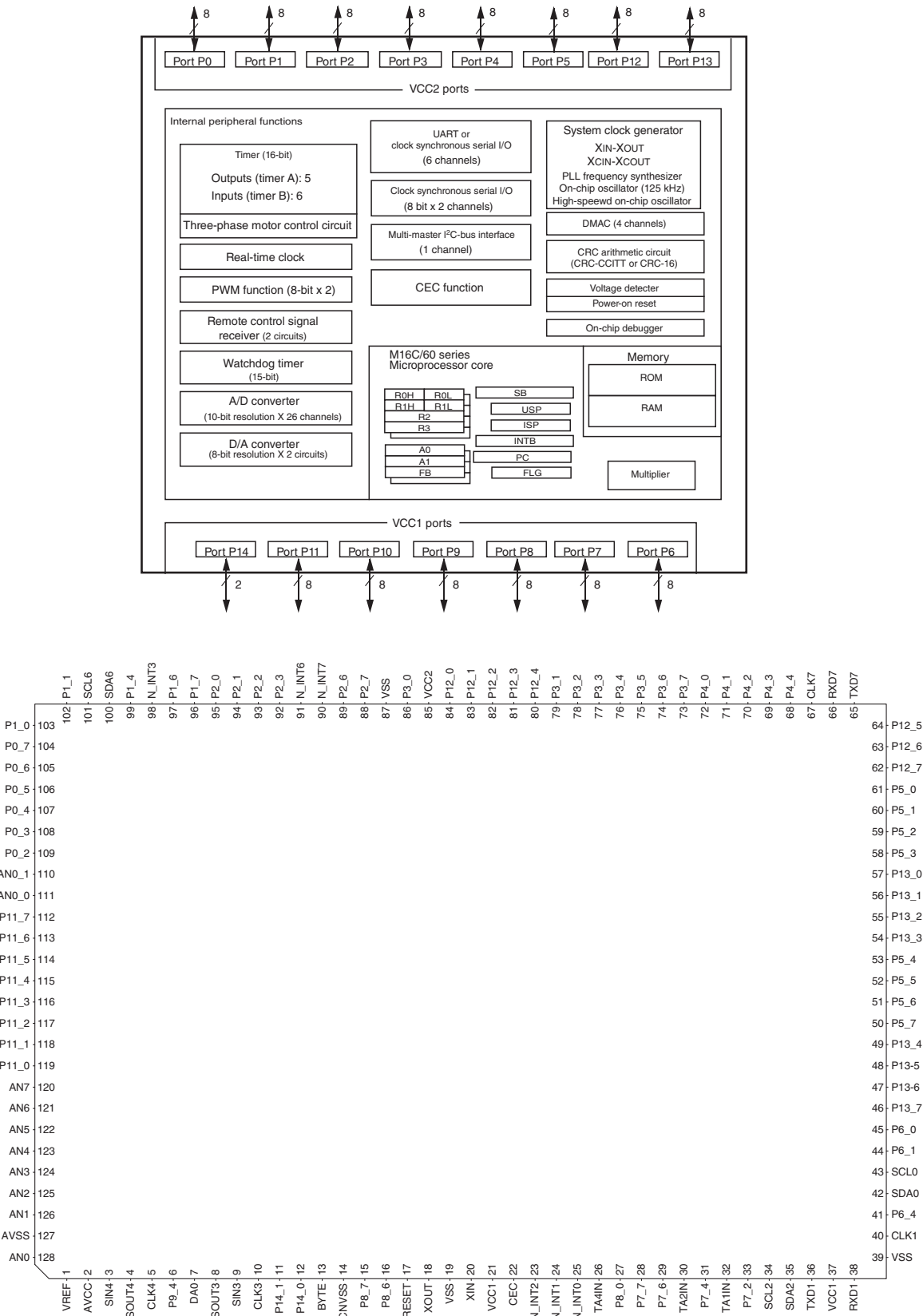
Pin No.	Function Name	I/O	Detail of Function
B15	TMS	I	JTAG mode select.
C14	TCK	I	JTAG clock.
A16	TDI	I	JTAG serial data input.
A15	TDO	O	JTAG serial data output.

Power Supply Pins

Pin No.	Function Name	Detail of Function	Pin No.	Function Name	Detail of Function
A6	VDD33	I/O power supply (+3.3 V).	K13	VSS	Ground (0 V).
E8			L6		
E9			L7		
E12			L8		
E13			L9		
F5			L10		
G5			L11		
H14			L12		
J14			L13		
K5			M6		
L5			M7		
M14			M8		
N14			M9		
P6			M10		
P7			M11		
P10			M12		
P11			M13		
D7			N6		
F6			N7		
F7			N8		
F8			N9		
F9	VSS	Ground (0 V).	N10		
F10			N11		
F11			N12		
F12			N13		
F13			B6		
G6			C6		
G7			R10	VPP	
G8			A2	VDD33USB	Power supply (+3.3 V) for USB interface. Ground (0 V).
G9			B2		
G10			A3	VSS33USB	
G11			B3		
G12			F3	VDD33PLL	Power supply (+3.3V) for PLL.
G13			G3	VSS33PLL	Ground (0 V).
H6			E6	VDD12	Power supply (+1.2V).
H7			E7		
H8			E10		
H9			E11		
H10			F14		
H11			G14		
H12			H5		
H13			J5		
J6			K14		
J7			L14		
J8			M5		
J9			N5		
J10			P8		
J11			P9		
J12			P12		
J13			P13		
K6	VDD12	Power supply (+1.2V).	D8	VDD12USB	Power supply (+1.2V) for USB interface.
K7			D1		
K8			C1	VSS12USB	Ground (0 V).
K9			H3	VDD12PLL	Power supply (+1.2V) for PLL.
K10			H2	VSS12PLL	Ground (0 V).
K11			G1	VDD12DCO	Power supply (+1.2V) for DCO.
K12			H1	VSS12DCO	Ground (0 V).

IC225: R5F3651TNFC (DIGITAL P.C.B.)
Microprocessor

* No replacement part available. / サービス部品供給なし



RX-V475/HTR-4066/
RX-V500D

Pin No.	Port Name	Function Name (P.C.B.)	I/O				Detail of Function
			FULL ON	PPWR OFF	MCU sleep	AC OFF	
1	VREF	VREF	MCU	MCU	MCU	MCU	AD standard voltage
2	AVCC	AVCC	MCU	MCU	MCU	MCU	Microprocessor power supply
3	SIN4	EEP_MISO	SI	SI	O	SI	EEPROM / Expansion Flash synchronization data input
4	SOUT4	EX_MOSI	SO	SO	O	SO	FL driver / EEPROM / Expansion Flash synchronization data input
5	CLK4	EX_SCK	SO	SO	O	SO	FL driver / EEPROM / Expansion Flash synchronous clock output
6	P9_4	+5EX_PON	O	O	O	O	
7	DA0	AMP_LMT	DA	O	O	O	Limiter control output
8	SOUT3	DSP_MOSI	SO	O	O	O	DSP, DIR, DAC synchronization data output
9	SIN3	DSP_MISO	SI	I-	I-	I-	DSP, DIR, DAC synchronization data input
10	CLK3	DSP_SCK	SO	O	O	O	DSP, DIR, DAC synchronous clock output
11	P14_1	HDMI_N_RST	O	O	O	O	HDMI RxTx reset
12	P14_0	TUN_N_RST	O	O	O	O	Tuner reset
13	BYTE	BYTE	MCU	MCU	MCU	MCU	Data bus width reshuffling input / Low: Single chip mode (16bit)
14	CNVSS	E8A_CNVSS	MCU	MCU	MCU	MCU	Processor mode select / Low: Single chip mode
15	P8_7	(no use)	O	O	O	O	(RX-V475/HTR-4066)
		DAB_PON	O	O	O	O	(RX-V500D)
16	P8_6	DIAG_FCT	O	O	O	O	Diag OK: Output High / Diag NG: Output Low (default)
17	/RESET	CPU_N_RST	MCU	MCU	MCU	MCU	Reset input
18	XOUT	XOUT	MCU	MCU	MCU	MCU	Oscillation circuit output
19	VSS	DGND	MCU	MCU	MCU	MCU	Microprocessor ground
20	XIN	XIN	MCU	MCU	MCU	MCU	Oscillation circuit input
21	VCC1	+3.3M	MCU	MCU	MCU	MCU	Microprocessor power supply
22	CEC	HDMI_CEC	IO	IO	I+	I+	Microprocessor CEC control
23	N_INT2	DSP_N_INT	IRQ	IRQ	IRQ	O	Interrupt input from DSP
24	N_INT1	HDMI_MUTE	IRQ	I-	I-	I-	HDMI MUTE input / H: Mute
25	N_INT0	HDMI_N_INT	IRQ	I-	I-	I-	Interrupt input from HDMI RxTx
26	TA4IN	DIR_N_INT	TMR	I	O	I	DIR interrupt input
27	P8_0	(no use)	O	O	O	O	
28	P7_7	DIR_N_RST	O	O	O	O	DIR reset
29	P7_6	DIR_N_CS	O	O	O	O	DIR chip select
30	TA2IN	TUN_N_INT	TMR	O	O	O	Tuner GPIO2 input
31	P7_4	NCPU_SPI_REQ	I	I	I	I	NET SPI request
32	TA1IN	ACPWR_DET	TMR	I+	I+	I+	AC power detection / L: Power down
33	P7_2	NCPU_SPI_RDY	I	I	I	I	NET SPI ready
34	SCL2	HDMI_SCL	SO	O	O	O	Video decoder, A-video switch I2C SCL output
35	SDA2	HDMI_SDA	SI	O	O	O	Video decoder, A-video switch I2C SDA input and output
36	TXD1	E8A_TXD	SO	SO	I+	I+	
37	VCC1	+3.3M	MCU	MCU	MCU	MCU	Microprocessor power supply
38	RXD1	E8A_RXD	SI	SI	I+	I+	
39	VSS	DGND	MCU	MCU	MCU	MCU	Microprocessor ground
40	CLK1	E8A_SCLK	SI	SI	I+	I+	
41	P6_4	E8A_BUSY	I-	I-	I-	I-	
42	SDA0	TUN_SDA	SI	O	O	O	Tuner I2C, Apple co-processor synchronization data input and output
43	SCL0	TUN_SCL	SO	O	O	O	Tuner I2C, Apple co-processor synchronous clock output
44	P6_1	(no use)	O	O	O	O	
45	P6_0	(no use)	O	O	O	O	
46	P13_7	VOL_MOSI	O	O	O	O	Electronic volume flip-flop synchronization data output
47	P13_6	VOL_SCK	O	O	O	O	Electronic volume flip-flop synchronous clock output
48	P13_5	I_PRT	I-	I-	I-	I-	Overcurrent protection detection
49	P13_4	TRANS_RY	O	O	O	O	
50	P5_7	DCDC_PON	O	O	O	O	
51	P5_6	MT_N_SW	O	O	O	O	Mute control (Subwoofer)
52	P5_5	E8A_N_EPM	I-	I-	I-	I-	

Pin No.	Port Name	Function Name (P.C.B.)	I/O				Detail of Function
			FULL ON	PPWR OFF	MCU sleep	AC OFF	
53	P5_4	HP_N_DET	I+	O	O	O	Headphone detection / L: Headphone detected
54	P13_3	HPRY	O	O	O	O	Headphone relay control
55	P13_2	SPRY_SB_BA	O	O	O	O	Speaker relay control (Surround back and Bi-Amp)
56	P13_1	(no use)					
57	P13_0	SPRY_5CH	O	O	O	O	Speaker relay control (Front / Center / Surround) / H: Relay ON
58	P5_3	MT_N_SB	O	O	O	O	Mute control (Surround back)
59	P5_2	(no use)	O	O	O	O	
60	P5_1	MT_N_5CH	O	O	O	O	Mute control (Front / Center / Surround)
61	P5_0	E8A_N_CE	I+	I+	I+	I+	
62	P12_7	OSDFS_N_CS	O	O	O	O	Chip select control of OSD Flash from microprocessor
63	P12_6	USB_VBUS_PON	O	O	O	O	
64	P12_5	PRY	O	O	O	O	Power relay control / H: On
65	TXD7	FPGA_MOSI	SO	SO	O	SO	FPGA, OSD Flash synchronization data output
66	RXD7	FPGA_MISO	SI	SI	O	O	FPGA, OSD Flash synchronization data input
67	CLK7	FPGA_SCK	SO	SO	O	SO	FPGA, OSD Flash synchronous clock output
68	P4_4	REM_OUT	O	O	O	O	Remote control code (spare)
69	P4_3	(no use)	I+	I+	I+	I+	
70	P4_2	(no use)	I+	I+	I+	I+	
71	P4_1	N_FCT	I	I	I	I	FCT detection / H: Product mode, L: FCT mode
72	P4_0	NDAC_N_MT	O	O	O	O	Mute control
73	P3_7		O	O	O	O	L: ROHM/FPGA SPI / H: Spalta OSD SPI
74	P3_6	VOL_RB	I+	I+	I+	I+	Volume rotary encoder B
75	P3_5	VOL_RA	I+	I+	I+	I+	Volume rotary encoder A
76	P3_4	FLD_N_CS	O	O	O	O	FL driver chip select
77	P3_3	FLD_N_RST	O	O	O	O	FL driver reset
78	P3_2	MIC_N_DET	I-	I-	I-	I-	MIC detection / L: MIC detected
79	P3_1	STBY_LED	O	O	O	O	Standby through LED / H: LED lighting
80	P12_4	NCPU_PON	O	O	O	O	H: Power supply ON
81	P12_3	DSP_PON	O				H: Power supply ON
82	P12_2	+3.3S_PON	O				H: Power supply ON
83	P12_1	HDMI_PON	O				H: Power supply ON
84	P12_0	VID_PON	O				H: Power supply ON
85	VCC2	VCC2	MCU	MCU	MCU	MCU	Microprocessor power supply
86	P3_0	EEP_N_CS	O	O	O	O	EEPROM chip select
87	VSS	VSS	MCU	MCU	MCU	MCU	Microprocessor ground
88	P2_7	MODE	I+	I+	I+	I+	+3.3V: Normal movement / 0V: MAC address writing permission
89	P2_6						(reserved)
90	N_INT7	REM_IN	IRQ	IRQ	IRQ	I	Remote control pulse input
91	N_INT6	PSW_N_DET	IRQ	IRQ	IRQ	I	Power system switch (Power, Scene) detection / L: Standby key ON
92	P2_3	DSP_N_RST	O	O	O	O	DSP reset
93	P2_2	DSP_N_RDY	I+	I+	O	I+	DSP Ready input
94	P2_1	DSP_N_CS	O	O	O	O	DSP chip select
95	P2_0	DSP_FMT	O	O	O	O	DSP full mute output / H: Mute
96	P1_7	PWM_PDN (reserved)	O	O	O	O	Digital amplifier power down control
97	P1_6	NCPU_VBUSDRV	I-	I-	I-	I-	USB power supply output requirement from NETWORK microprocessor
98	N_INT3	MHL_WAKE					(reserved)
99	P1_4	PWM_N_RST (reserved)	O	O	O	O	Digital amplifier reset
100	TXD6	NCPU_SPI_MOSI	SO	O	O	O	NET SPI data output
101	RXD6	NCPU_SPI_MISO	SI	O	O	O	NET SPI data input
102	CLK6	NCPU_SPI_SCK					NET SPI clock output
103	P1_0	NCPU_SPI_N_CS	O	O	O	O	NET SPI chip select

Pin No.	Port Name	Function Name (P.C.B.)	I/O				Detail of Function
			FULL ON	PPWR OFF	MCU sleep	AC OFF	
104	P0_7	DAC_N_CS	O	O	O	O	DAC chip select
105	P0_6	NCPU_AMUTE	I	O	O	O	NET audio mute demand
106	AN0_5	PS3_PRT	AD				PS protection detection 3
107	AN0_4	PS2_PRT	AD				PS protection detection 2
108	AN0_3	L3_DET	AD	I	I	I	D terminal L3 detection
109	AN0_2	USB_VBUS_PRT	AD	I	I	I	USB iPad power supply feedback
110	AN0_1	THM3	AD	I	I	I	Temperature detection 3
111	AN0_0	DEST	AD	I	I	I	Model distinction
112	P11_7	NCPU_N_RST	O	O	O	O	
113	P11_6	DIR_SDO	I	I	O	I	DIR_SDO input for CDDA writing
114	P11_5	DIR_WCK	I	I	O	I	DIR_WCK input for CDDA writing
115	P11_4	TUNI2C_ON	O	O	O	O	(reserved) I2C switching to Tuner
116	P11_3	VIDI2C_ON	O	O	O	O	Vdec and A-video selector I2C line control
117	P11_2	MHL_CD_IN5	I	I	I	I	MHL cable detection
118	P11_1	MHL_VBUS_N_PRT	I	I	I	I	MHL VBUS overcurrent detection
119	P11_0	MHL_VBUS_PON	O	O	O	O	MHL VBUS control
120	AN7	DC_PRT	AD	I	I	I	Power amplifier DC detection
121	AN6	AMP_OLV	AD	I	I	I	Power amplifier output level detection
122	AN5	THM1	AD	I	I	I	Temperature detection 1
123	AN4	THM2	AD	I	I	I	Temperature detection 2
124	AN3	KEY2	AD	I	I	I	KEY AD value uptake 2
125	AN2	KEY1	AD	I	I	I	KEY AD value uptake 1
126	AN1	PS1_PRT	AD	I	I	I	PS protection detection 1
127	AVSS	AVSS	MCU	MCU	MCU	MCU	Microprocessor ground
128	P10_0	(no use)	O	O	O	O	AD spare

Key detection for A/D port

Key input (A/D) pull-up resistance: 10 k-ohms

	0 Ω	+ 1.0 kΩ	+ 1.0 kΩ	+ 1.5 kΩ	+ 1.5 kΩ	+ 2.2 kΩ	+3.3 kΩ	+ 4.7 kΩ	+ 13.2 kΩ	+ 22 kΩ	+ 33 kΩ
Detected voltage value at 125 pin	0 – 0.15 V	0.15 – 0.425 V	0.425 – 0.703 V	0.703 – 0.978 V	0.978 – 1.241 V	1.241 – 1.536 V	1.536 – 1.84 V	1.84 – 2.102 V	2.102 – 2.299 V	2.336 – 2.55 V	2.55 – 2.971 V
A/D value (3.3 V=255)	0 – 11	12 – 32	33 – 54	55 – 75	76 – 96	97 – 119	120 – 142	143 – 163	163 – 177	182 – 197	198 – 229
KEY1	RADIO (SCENE4)	NET (SCENE3)	TV (SCENE2)	BD/DVD (SCENE1)	—	—	INPUT >	INPUT <	—	(power)	TONE CONTROL

	0 Ω	+ 1.0 kΩ	+ 1.0 kΩ	+ 1.5 kΩ	+ 1.8 kΩ	+ 2.2 kΩ	+3.3 kΩ	+ 4.7 kΩ	+ 6.8 kΩ	+ 10 kΩ	+ 22 kΩ	+ 68 kΩ
Detected voltage value at 124 pin	0 – 0.15 V	0.15 – 0.425 V	0.425 – 0.703 V	0.703 – 0.999 V	0.999 – 1.279 V	1.279 – 1.564 V	1.564 – 1.86 V	1.86 – 2.142 V	2.142 – 2.399 V	2.399 – 2.653 V	2.653 – 2.919 V	2.916 – 3.175 V
A/D value (3.3 V=255)	0 – 11	12 – 32	33 – 54	55 – 77	78 – 99	100 – 121	122 – 144	145 – 166	167 – 186	187 – 205	206 – 226	227 – 246
KEY2	DIRECT	TUNING >>	TUNING <<	AM (RX-V475/HTR-4066) DAB (RX-V500D)	FM	PRESET >	PRESET <	MEMORY	INFO	STRAIGHT	PROGRAM >	PROGRAM <

Destination detection for A/D port

Pull-up resistance: 10 k-ohms

R5419 on OPERATION P.C.B.	0 Ω	1.2 kΩ	2.7 kΩ	4.7 kΩ	6.8 kΩ	10 kΩ	15 kΩ	47 kΩ	100 kΩ
Detected voltage value at 111 pin	0 – 0.162 V	0.162 – 0.517 V	0.517 – 0.872 V	0.872 – 1.193 V	1.193 – 1.492 V	1.492 – 1.816 V	1.816 – 2.2 V	2.572 – 2.869 V	2.869 – 3.163 V
A/D value	000	111	222	333	444	555	666	777	888
Destination	J	U	C	R, S	T	K	A	B, G, F	L, H

PIN CONNECTION DIAGRAMS

ICs

A3V56S30FTP-G6 	BA4560F-E2 	D70YE101BRFP266 	DM860A-AQE
74LVC08APW 	BD3473KS2 	BD9328FJ 	
KIA7805API KIA7812API 	KIA7912PI 	LAN8700C-AEZG-TR 	LM19CIZ/LF
M66003-0131FP-R 	MFI337S3959 	MX29GL256FLT2I-90Q 	MX29LV160DBTI-70G
NJM2388F33 	NJM41033V (TE2) 	NJM4565M (TE1) 	NJCW1329FH3
PCM9211PTR 	SII9573CTUC 	R1172H121D-T1-F R1172H501D-T1-F 	R1EX25032ATA00A
R1163N501B-TR-FE 	R1171S501B-E2-FE 	R5F3651TNFC 	RP130Q331D-TR-F RP130Q501D-TR-F
		SN74LVC1G17DCKR 	

ICs

STR2A153 	TC74LCX245FT 	TC74VHCU04FT 	TC7MBL3257CFK 	TC7WH125FK TC7WH126FK 	TL431ACLPR 	W25Q16CVSSIG
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Diodes

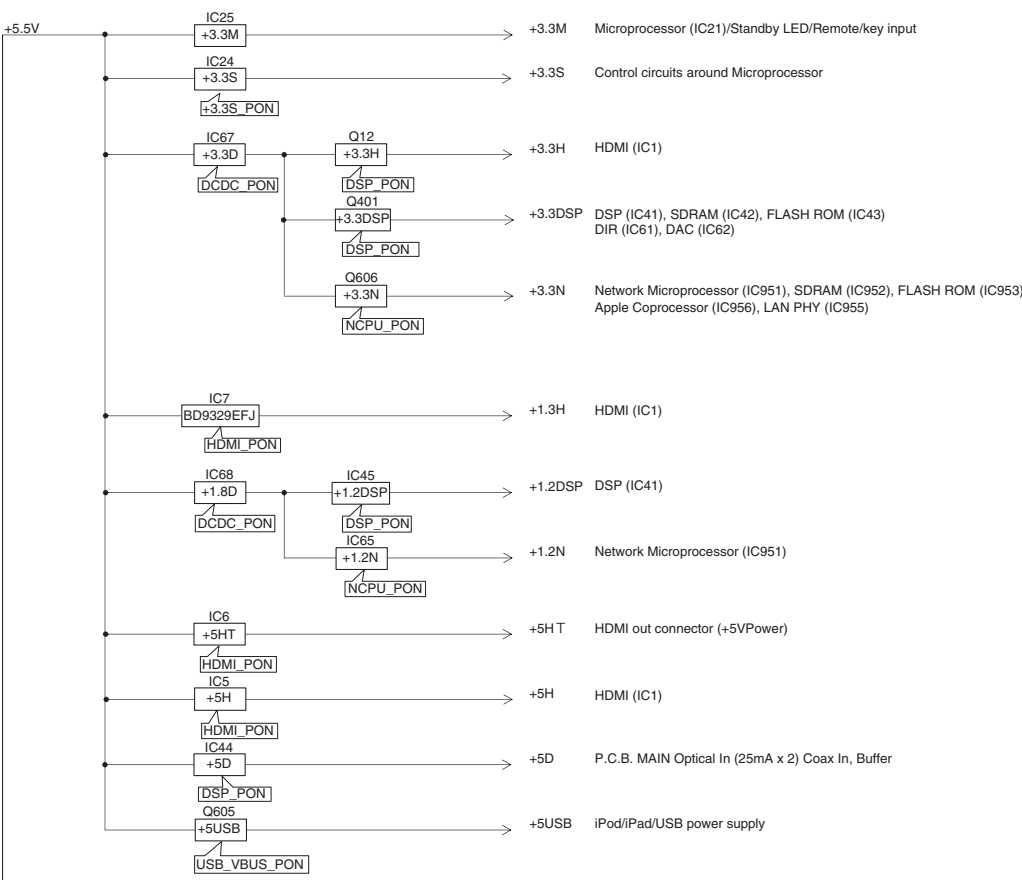
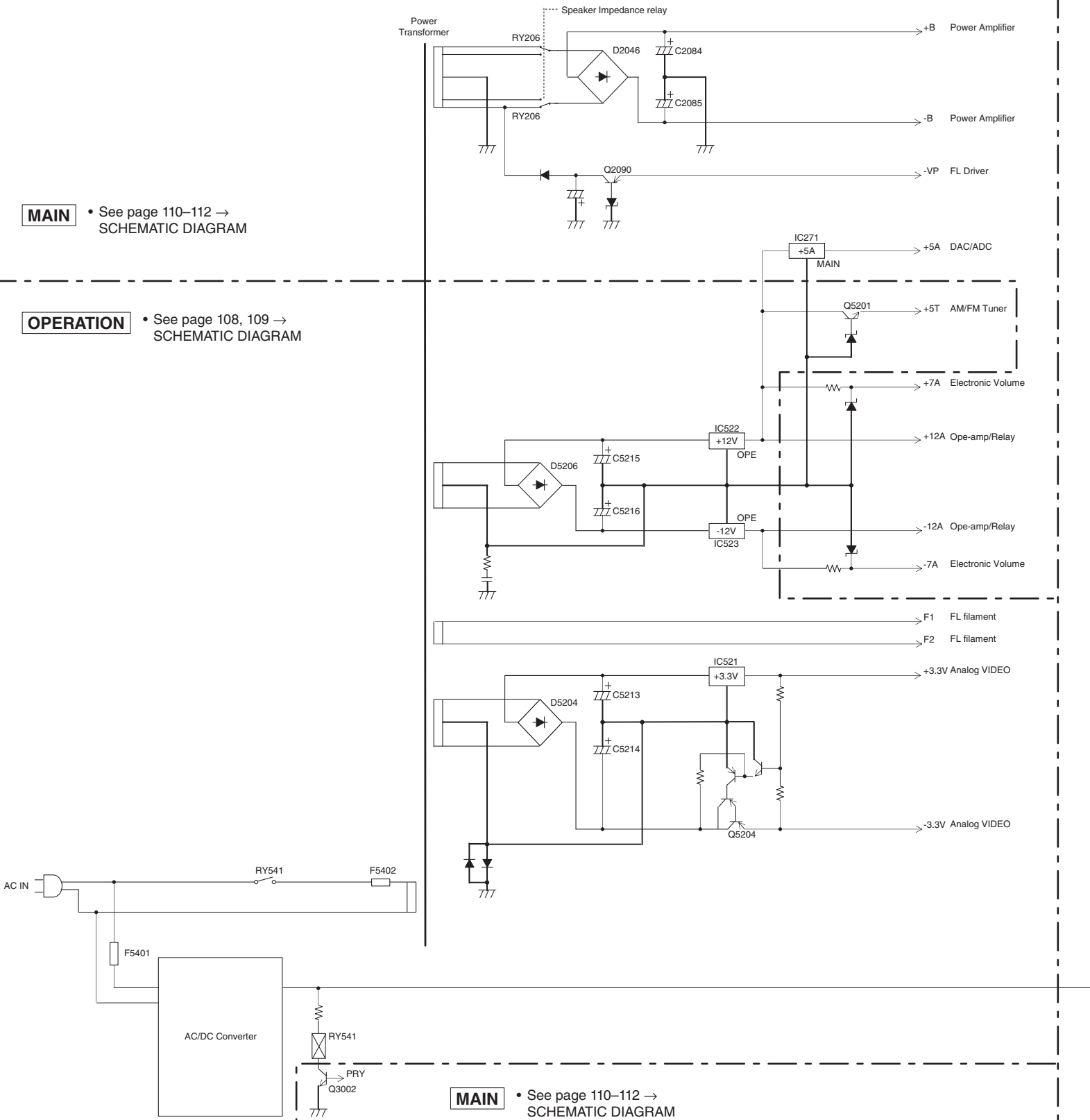
1N4003S 	1SS355VMTE-17 	DBL155G 	RB051L-40 	RB215T-90 	RB500V-40 RB501V-40 RB521S-30 	RF101L2STE25
RS203M-B-C-J80 	SARS05 	TFZGTR6.8C 	TS6P03G 6.0A 200V 	UDZS39B TE-17 39V UDZV12B UDZV13B UDZV3.9B UDZV4.3B UDZV5.1B UDZV5.6B 		

Transistors

2N5401C-AT/P 	2N5551C-AT 	2SA1162-Y (TE85R, F) 	2SA1312-GR,BL 	2SA1576UBTLR 	2SA1708 2SC4488 	2SA949 2SC2229
2SC2713-GR 	2SC4081UBTLR 	2SC4115S 	2SD2704 K 	DTA044EUBTL DTC014EUBTL DTC044EUBTL 		HN4B01JE
KRA104S-RTK KRC102S-RTK KRC104S-RTK 	KTA1046-Y-U/PFY KTA1659A-U/PF 	KTC3198 Y AT 	KTC3875S 	RAL035P01 	μPA672T-T1-A 	



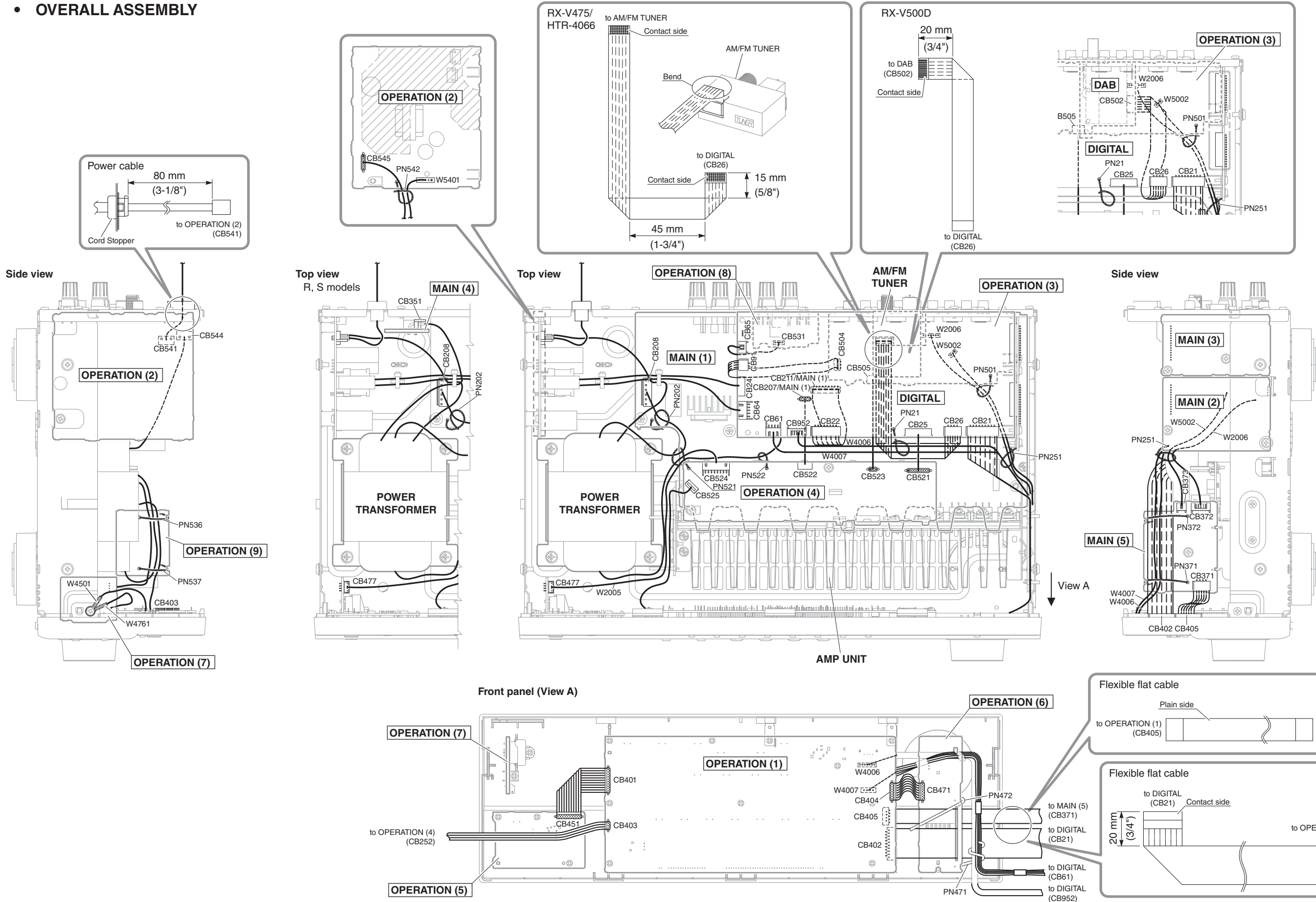
Power Supply Section Block Diagram



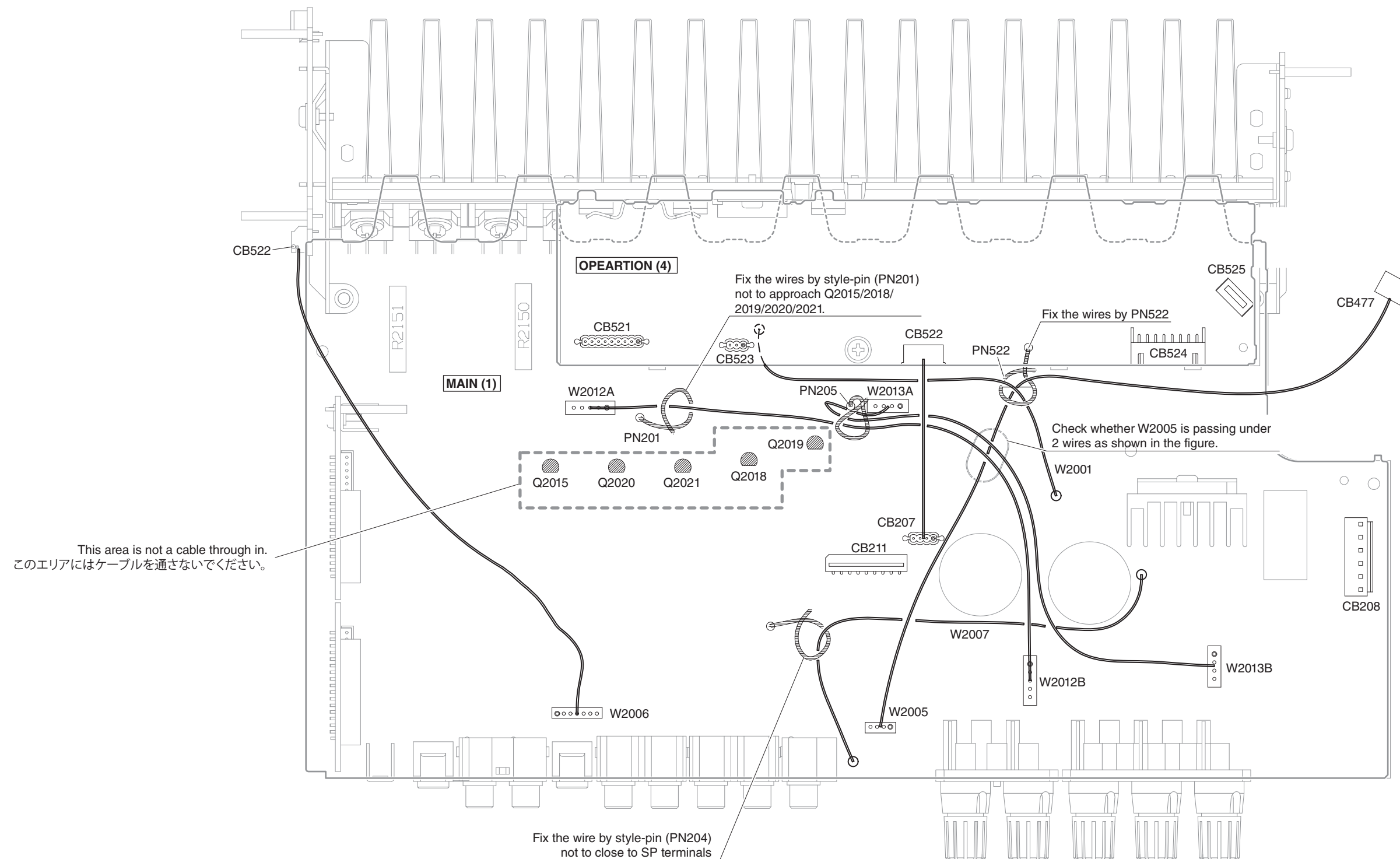
DIGITAL • See page 103–107 → SCHEMATIC DIAGRAM

■ WIRING DIAGRAMS

- OVERALL ASSEMBLY



- AMP UNIT



PRINTED CIRCUIT BOARDS

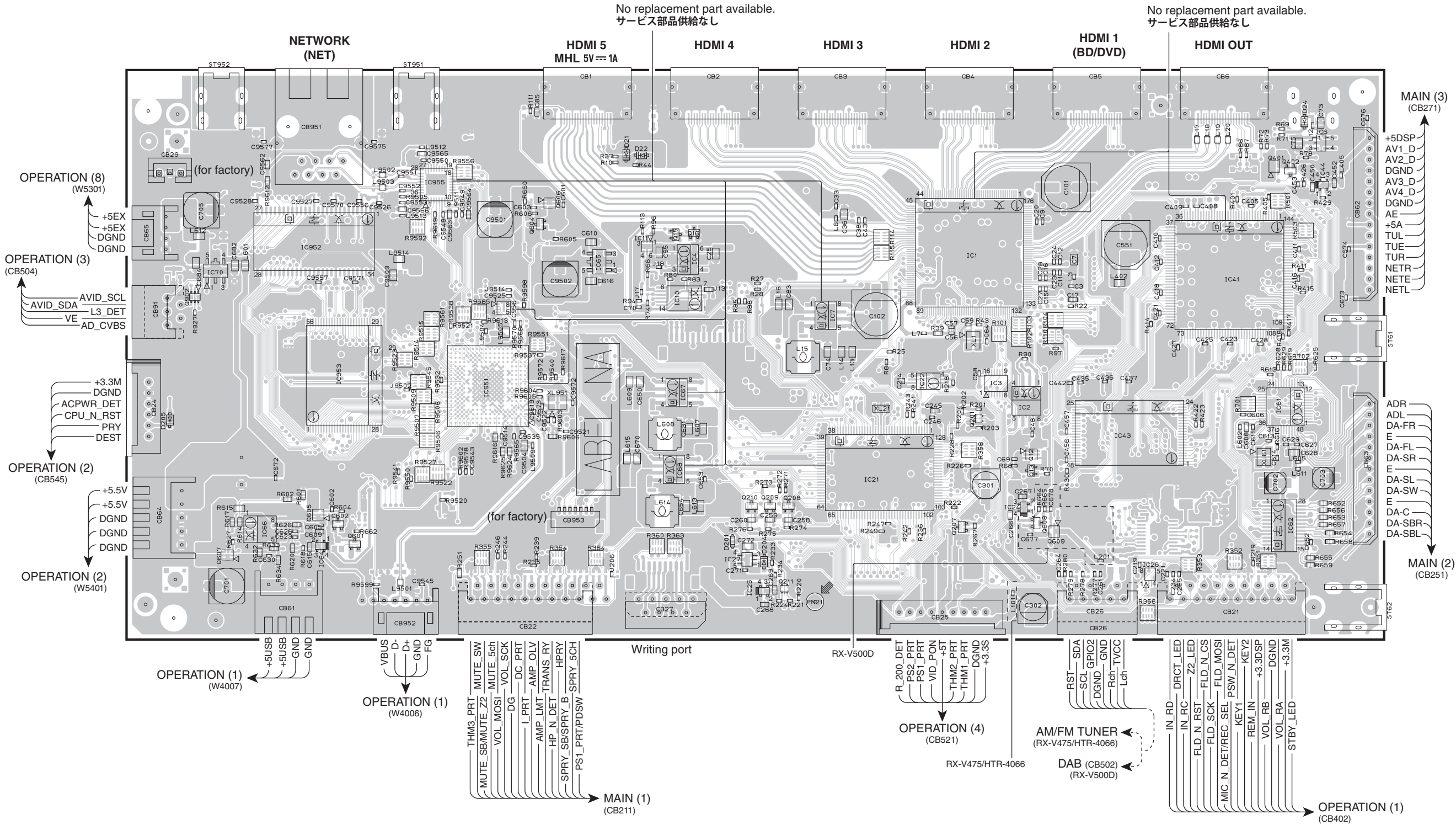
RX-V475/HTR-4066

RX-V500D

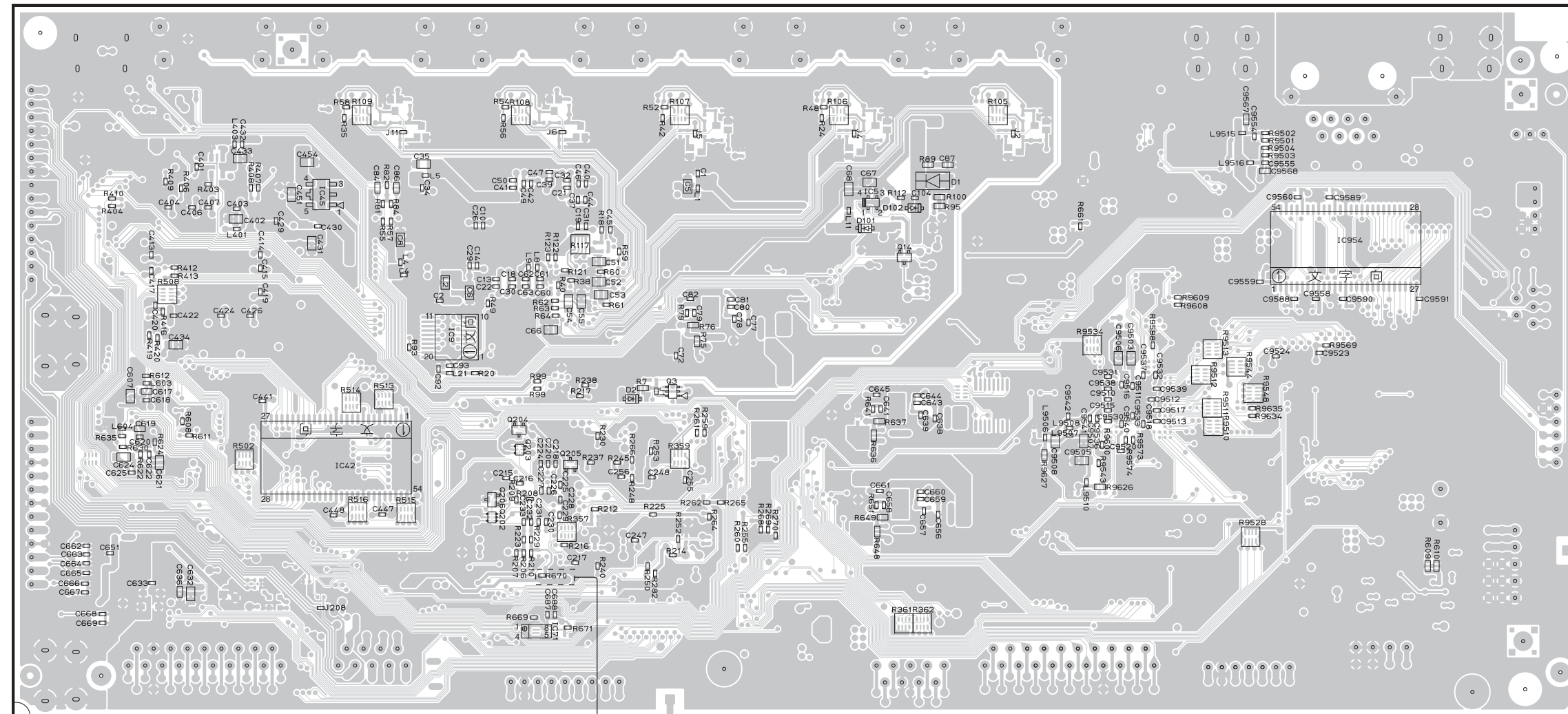
• Semiconductor Location

Ref no.	Location	Ref no.	Location	Ref no.	Location	Ref no.	Location	Ref no.	Location	Ref no.	Location	Ref no.	Location	Ref no.	Location	Ref no.	Location
D21	E3	D205	B4	IC6	I3	IC22	G4	IC41	H4	IC64	C5	IC70	B4	IC956	D4	Q201	G4
D22	E3	IC1	G3	IC7	F4	IC24	G5	IC43	H5	IC65	E3	IC951	D4	Q12	G5	Q207	G5
D24	I3	IC2	G4	IC10	E4	IC25	F5	IC44	I3	IC66	C5	IC952	C3	Q13	G5	Q208	F5
D201	E5	IC3	G4	IC11	E3	IC26	H5	IC61	I4	IC67	E4	IC953	C4	Q15	E3	Q209	F5
D204	F5	IC4	E3	IC21	F5	IC27	E5	IC62	I5	IC68	E5	IC955	D3	Q16	E3	Q210	F5

DIGITAL (Side A)



DIGITAL (Side B)



RX-V500D

- Semiconductor Location

Ref no.	Location
D1	F3
D2	D4
D101	E3
D102	F3
IC5	E3
IC9	C4
IC42	C5
IC45	C3
IC71	D5
IC954	H3
Q3	D4
Q14	E4
Q202	D5
Q203	D4
Q204	D4
Q205	D5
Q206	D5

OPERATION (4)
(CB525)

